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Accurate spectral test algorithms with relaxed instrumentation requirements

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Accurate spectral test algorithms with relaxed instrumentation requirements

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DEDICATION

This work is dedicated to my wife Yenumula Vanaja for staying with me throughout the course of PhD with patience and love and to my dad Sri Sudani Satyanarayana and my mother Smt. Sudani Bala Kumari for believing in me and sending me abroad to pursue my PhD.

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ABSTRACT

Spectral testing is widely used to test the dynamic linearity performance of Analog-to-Digital Converters (ADC) and waveform generators. Dynamic specifications for ADCs are very important in high speed applications such as digital communications, ultrasound imaging and instrumentation. With improvements in the performance of ADCs, it is becoming an expensive and challenging task to perform spectral testing using standard methods due to the requirement that the test instrumentation environment must satisfy several stringent conditions. In order to address these challenges and to decrease the test cost, in this dissertation, three new algorithms are proposed to perform accurate spectral testing of ADCs by relaxing three necessary conditions required for standard spectral testing methods. The testing is done using uniformly sampled points.

The first method introduces a new fundamental identification and replacement (FIRE) method, which eliminates the requirement of coherent sampling when using the DFT for testing the spectral response of an ADC. The robustness and accuracy of the proposed FIRE method is verified using simulation and measurement results obtained with non-coherently sampled data.

The second method, namely, the Fundamental Estimation, Removal and Residue Interpolation (FERARI) method, is proposed to eliminate the requirement of precise control over amplitude and frequency of the input signal to the ADC. This method can be used when the ADC output is both non-coherently sampled and clipped. Simulation and measurement results using the FERARI method with non-coherently sampled and clipped outputs of the ADC are used to validate this approach.

A third spectral test method is proposed that simultaneously relaxes the conditions of using a spectrally pure input source and coherent sampling. Using this method, the spectral characteristics of a high resolution ADC can be accurately tested using a non-coherently sampled output obtained with a sinusoidal input signal that has significant and unknown levels of nonlinear distortion. Simulation results are presented that show the accuracy and robustness of the proposed method.

Finally, the issue of metastability in comparators and Successive Approximation Register (SAR) ADCs is analyzed. The analysis of probability of metastability in SAR ADCs with and without using metastable detection circuits is provided. Using this analysis, it is shown that as the frequency of sampling clock increases, using a metastable detection circuit decreases the probability of metastability in SAR ADCs.

CHAPTER I

INTRODUCTION

In this dissertation, methods for accurate spectral testing with relaxed requirements on test setup instrumentation are presented. The proposed methods are compared with standard test methods such as the IEEE standard that is widely used throughout the industry, windowing techniques, and the four parameter sine fitting method. It is shown that the proposed methods can accurately perform spectral testing even after relaxing some of the stringent (and expensive) conditions that are required for standard testing approaches. The methods are applicable for high performance Analog-to-Digital Converter (ADC) testing and high performance waveform generator testing. In the next three chapters, three methods are presented that perform spectral testing with accuracy and efficiency.

In this chapter, motivation to perform low-cost testing is provided followed by an overview of the IEEE standard method to perform spectral test. The challenges involved in performing spectral testing of high performance ADCs and a brief summary about the organization of this dissertation are presented.

I. MOTIVATION

Modern device technology requirements and advancements in semiconductor processing technologies are causing the density of gates in a silicon wafer to continuously grow at a rapid rate. This rapid growth is widely viewed as the trend in the semiconductor industry predicted by Moore's law. This enables designers to

economically and efficiently design a system with several high-complexity functional blocks on a single chip, often called System-on-Chip (SoC) [1]. The performance of stand-alone parts has also been increasing with developments in semiconductor technology. However, this increase in performance of stand-alone parts and increases in size and complexity in the design of SoCs has introduced several significant challenges for testing the parts or systems.

Production testing of stand-alone parts is performed to examine if the part meets a set of design specifications or performance requirements. The part is marked as a good part or a bad part depending on the positive or negative outcome of the production test. With increases in the performance of stand-alone parts, it is becoming a challenge to economically procure high accuracy test equipment to perform conventional tests. Paralleling this challenge are dramatic increases in the cost of testing. Therefore, there is an imminent need to develop new test methods that can reduce test costs by using low-end measurement setups to accurately test high performance parts.

SoCs are gaining popularity and becoming more favorable for production as they decrease the design cost by allowing the whole system to be designed on a single chip. SoCs are typically comprised of several complex sub circuits and it is usually essential to individually test all sub circuits in the system to guarantee the specified system performance. It is challenging to de-embed each block separately for testing the sub circuits on the SoC due to dense integration and local loading and this further leads to increases in test costs. One solution to testing SoCs cost effectively is to use Built-in Self-Test (BIST) circuits. When BIST is employed, the test circuitry is also present on

the same chip as the Device under Test (DUT). With a BIST solution, the challenges associated with de-embedding each block can be reduced or eliminated. However, economical constraints dictate that the test circuitry in BIST circuits should have negligible area compared to that of the DUT. If conventional test methods are used in BIST circuits for testing analog functions, the test circuitry often must include high accuracy, spectrally pure, or high linear stimulus signal generators. These high-performance signal generators invariably necessitate a substantial design effort and require a large area. In some cases, the area required by the test circuitry could be more or even much more than that of the DUT. In almost all applications, a large area requirement for BIST circuits would be unacceptable. As a result, for BIST circuits to be practical, new test methods need to be developed that can relax the conditions on test setup measurement so that low-end measurement systems can be designed on-chip and still provide accurate test results. The *International Technology Roadmap for Semiconductors* also recognizes the need and suggested that more research needs to be done on BIST for analog and mixed-signal circuits.

Analog-to-Digital Converters are one of the most widely used integrated circuits. They are not only used as stand-alone parts but are also widely used in the analog front end in SoCs [2]. ADCs are usually tested for static parameters such as Integral Non-linearity (INL), Differential Non-linearity (DNL), offset, gain, etc. They are also tested for dynamic parameters such as Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR), Signal to Noise Ratio (SNR), etc. [3].

Conventional data converter testing methods have changed little over the past three decades. When these testing methods evolved, the performance of the best ADCs available from industry was modest by today's standards and the cost of computing equipment and computing time was very high. As a consequence, a good testing solution at the time was based upon using a reasonably good signal generator and minimal post-processing of measurement data by a computer. In the intervening three decades there have been dramatic changes in both performance and cost structures. The performance of ADCs has dramatically increased, the cost of high-end analog test equipment used to generate test signals for testing ADCs has increased dramatically, but the cost of computational equipment and computational operations has dropped at a much higher rate. So, the question naturally arises, about whether new methods for testing high performance ADCs that are no longer constrained by the cost of computational equipment and computational operations can be developed that can modestly or even dramatically reduce the cost of testing high performance ADCs.

To decrease the test cost of ADCs, new methods are needed that can decrease the measurement setup cost by relaxing the stringent conditions required for conventional instruments used for testing ADCs and, if necessary, increasing or dramatically increasing the use of computational tools as a part of the testing flow. In [4], a Stimulus Error Identification and Removal (SEIR) method was proposed that can relax the requirement of high linear stimulus to perform static Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) linearity testing. With the SEIR approach, a tradeoff was made between linearity of the stimulus signal and the number of computational

operations that can provide a dramatic overall reduction in test costs. In this dissertation, work has been done to relax three stringent conditions (on the test setup) that are required to perform accurate dynamic spectral testing of an ADC and these three conditions are the major contributors to the high test costs with conventional testing approaches. Paralleling the relaxation of the performance requirements for the signal generator has been a significant increase in the computational complexity of the testing algorithm. But as with the SEIR approach, the tradeoffs between test equipment specifications and computational time will provide a dramatic overall reduction in spectral testing costs in today's environment.

It should be noted here that the focus in this dissertation on ADC testing has been chosen only for convenience. The same methods can also be used to perform spectral testing of waveform generators.

Dynamic testing of ADCs is often called spectral testing or AC testing and includes testing of the ADCs dynamic (frequency dependent) specifications. In contrast, full spectrum testing not only tests dynamic specifications but also focuses on testing all spectral bins including harmonic and non-harmonic bins. Being able to perform full spectrum testing is especially important for systems whose Spurious Free Dynamic Range (SFDR) is limited by non-harmonic spurious tones, such as time-interleaved ADCs. The test setup for both spectral test and full spectrum test is the same.

II. IEEE STANDARD ADC SPECTRAL TEST

The IEEE standard for Digitizing Waveform Recorders (IEEE Std. 1057) [5] and IEEE standard for Terminology and Test Methods for Analog-to-Digital Converters (IEEE Std. 1241) [6] specifies that the test setup should satisfy the following five conditions for accurately performing the spectral testing of ADCs. Firstly, the spectral purity of the input signal to ADC should be about 3 to 4 bits more pure than the ADC under test. In other words, to test an N-bit ADC, the input signal should be more than N+3 bits pure. The second condition is that the peak-to-peak voltage of the input signal should be slightly lower than the ADC input range so that the output of the ADC is not clipped. The third condition is to have very low relative jitter between the clock and input signals. The fourth condition is that, if possible, the input signal be coherently sampled. Finally, the total number of sampled points (or data record length) should be sufficiently large.

Fig. 1.1 shows the recommended test setup for standard spectral testing of an N-bit ADC. The setup consists of a master clock that controls the frequency of both the clock signal and the input signal. This can provide coherent sampling. Occasionally, there is a filter present between the input signal source and the ADC under test. The filter is added to improve the spectral purity of the input signal to the ADC. The amplitude of the input signal is selected such that the peak-to-peak value of input to ADC is within the ADC input range. Care is also taken to obtain very small relative jitter between the input and clock signals using low jitter clock generators. Using this setup, the output of ADC is

acquired and analyzed for spectral parameters of the ADC under test. In this section, it is considered that all the above conditions are satisfied.

Let f_{Sig} be the frequency of input signal, f_{Samp} be the clock frequency, M be the total number of data points recorded to measure the spectral characteristics and J be the total number of periods of the input signal sampled in the recorded data. The four parameters are related by equation (1.1).

$$J = M \frac{f_{Sig}}{f_{Samp}} \tag{1.1}$$

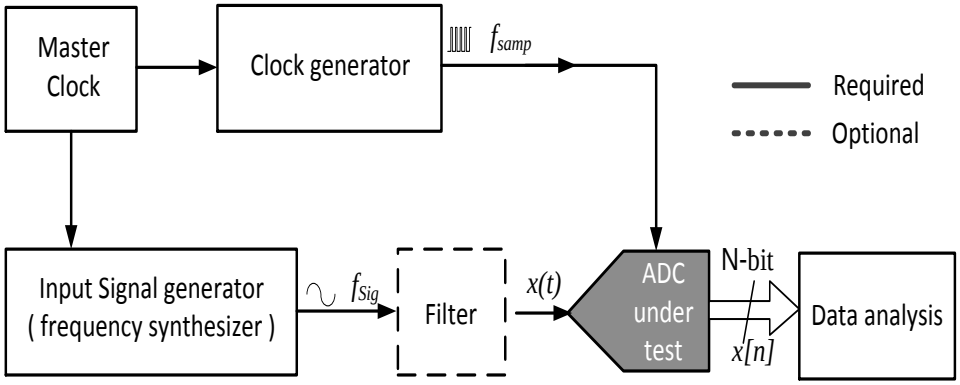

Figure 1.1: Setup to test ADC Spectral characteristics

The sampling is said to be coherent if J in (1.1) is an integer that is co-prime with M and non-coherent if J is a non-integer. In addition, it is recommended that $J > 5$ [6].

It is recommended to perform coherent sampling to accurately test an ADC. Fig. 1.2 shows the spectrum of an example ADC when sampled coherently. It can be seen from Fig. 1.2 that the spectrum is clean and all the spectral parameters such as, THD, SFDR and SNR, can be accurately estimated as explained below.

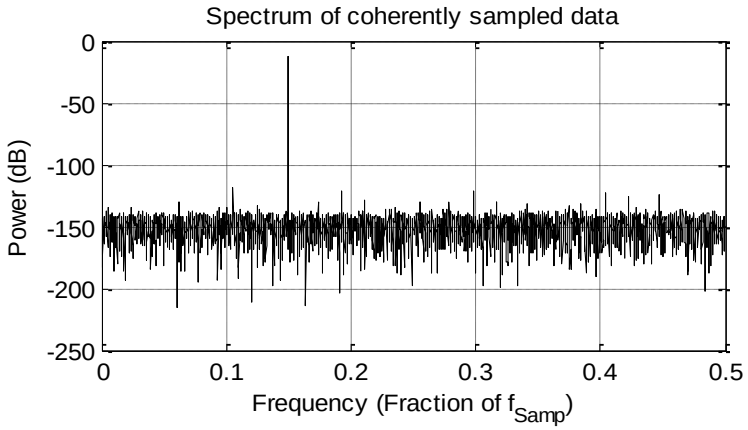

Figure 1.2: Power Spectrum of a coherently sampled ADC Output

Assume *x(t)* is the time domain representation of the analog input signal. The signal is ideally a pure sine wave and is given by equation (1.2).

$$x(t) = A\cos\left(2\pi f_{Sig} t\right) \tag{1.2}$$

where, *A* is the amplitude of *x(t)*.

Let *x[n]* be the analog interpretation of the digital output obtained from the ADC whose gain error and offset have been calibrated. *x[n]* can be represented by (1.3).

$$x[n] = A\cos\left(\frac{2\pi J}{M} n + \phi\right) + \sum_{h=2}^{H} A_h \cos\left(\frac{2\pi hJ}{M} n + \phi_h\right) + w[n] \tag{1.3}$$

for n = 0,1,2,….,*M*-1. ϕ is the initial phase of the sampled *x(t)*. *M* is usually selected to be a power of 2 for faster processing of the Discrete Fourier Transform (DFT) with the Fast Fourier Transform (FFT) algorithm. *H* is the total number of harmonics considered in *x[n]*, A_h and ϕ_h are the amplitude and initial phase of h^{th} harmonic respectively. It is assumed that $A_h << A$ and $\phi_h \in [0,2\pi)$ for all $2 \le h \le H$. *w[n]* corresponds to white noise

in n^{th} sample which can be due to quantization noise, input referred ADC noise and additive noise in the input signal. The harmonics in the output of ADC, *x[n]*, are attributable to the distortion of ADC. Actually, there are an infinite number of harmonics. But, for analysis purposes, only the first H harmonics are considered throughout this dissertation. This is a justifiable assumption since the higher order harmonics in a real ADCs usually have negligible power.

The spectral parameters can be accurately obtained by taking DFT of *M* coherently sampled data points. The DFT of *x[n]* is given by equation (1.4).

$$X_k = \frac{1}{M}\sum_{n=0}^{M-1} x[n] e^{-j\frac{2\pi k}{M}n}, \text{ for } k = 0,1,2,...,M-1 \tag{1.4}$$

where *k* represents the frequency bin's index. For example, with coherent sampling, $k = h*J$ represents the frequency bin of the h^{th} harmonic and if $h = 1$, $k = J$ represents the frequency bin of the fundamental. X_0 corresponds to the DC component in signal *x[n]*. Other values of *k* correspond to noise.

From equations (1.3) and (1.4), neglecting the effect of noise, X_k can be rewritten and given as (1.5).

$$X_k = \left(\begin{array}{l} \dfrac{A}{2M}\left\{ \dfrac{\sin\left(\pi\left(J-k\right)\right)}{\sin\left(\dfrac{\pi\left(J-k\right)}{M}\right)} e^{j\left(a\left(J-k\right)+\phi\right)} + \dfrac{\sin\left(\pi\left(J+k\right)\right)}{\sin\left(\dfrac{\pi\left(J+k\right)}{M}\right)} e^{-j\left(a\left(J+k\right)+\phi\right)} \right\} \\ +\sum_{h=2}^{H} \dfrac{A_h}{2M}\left\{ \dfrac{\sin\left(\pi\left(hJ-k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ-k\right)}{M}\right)} e^{j\left(a\left(hJ-k\right)+\phi_h\right)} + \dfrac{\sin\left(\pi\left(hJ+k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ+k\right)}{M}\right)} e^{-j\left(a\left(hJ+k\right)+\phi_h\right)} \right\} \end{array} \right) \tag{1.5}$$

It can be seen from (1.5) that, for coherent sampling,

$$X_J = \frac{A}{2} e^{j\phi} \quad \text{and} \quad X_{hJ} = \frac{A_h}{2} e^{j\phi_h} \tag{1.6}$$

For other values of k, X_k represents the noise as there is no contribution from the fundamental and harmonics on the bins if the M points are coherently sampled. The power of fundamental, h[th] harmonic and noise in coherently sampled data can be accurately estimated as P_1, P_h and P_{noise} respectively using (1.7),

$$P_1 = 2\left|X_J\right|^2 = \frac{A^2}{2}; \qquad P_h = 2\left|X_{hJ}\right|^2 = \frac{A_h^2}{2}; \qquad P_{noise} = \sum_{\substack{k=1 \\ k\neq J,hJ \\ h=2,3,..,H}}^{M-1} \left|X_k\right|^2 \tag{1.7}$$

From (1.7), the spectral parameters such as THD, SNR and SFDR for a coherently sampled signal can be calculated using equations in (1.8).

$$THD = \frac{\sum_{h=2}^{H} P_h}{P_1}; \qquad SNR = \frac{P_1}{P_{noise}}; \qquad SFDR = \frac{P_1}{2 * \max\limits_{\substack{k=1,..,M/2 \\ k\neq J}} \left(\left|X_k\right|^2\right)} \tag{1.8}$$

The equations (1.6-1.8) give accurate values of spectral parameters. Also, since the power of each frequency bin can be obtained accurately, this coherent sampling method can be used for full spectrum testing.

The challenges in performing high performance ADC spectral test using standard methods are discussed in the following section.

III. CHALLENGES IN ADC SPECTRAL TEST

As mentioned in section I, there are five conditions that need to be satisfied to perform standard ADC spectral testing. It can be said that the first four conditions are challenging to achieve as the performance of ADC continuously increases.

The first condition is to use a very highly pure sinusoid signal source as input to the ADC under test. This condition requires either new methodologies to design highly pure signal sources or several filters to suppress the unwanted harmonics. Both solutions lead to high test cost. Also, as noted earlier, for BIST ADCs, the area required to design highly linear signal sources could be very large leading to high costs.

The second condition is to be able to control the amplitude so that the peak-to-peak voltage of the input signal is within the input range of the ADC. This condition could be a challenging task in BIST circuits as precise control over amplitude of the signal is not possible. With trend shifting towards designing BIST ADCs, it is important to be able to test the ADC characteristics from clipped output data.

The next condition is to have minimal relative jitter between the input signal and the clock signal. This requires high accuracy clock and signal generators, which could increase the test cost with increase in ADC performance.

The fourth condition is to sample the input signal coherently. Achieving coherent sampling is one of the major bottlenecks in performing spectral testing. In order to achieve coherent sampling, it is required to use high accuracy signal generators or Phase Locked Loops (PLL). This results in additional hardware which adds to the total ADC test cost. Also, in BIST applications, it is impractical to achieve coherent sampling as PLLs or high accuracy frequency synthesizers cannot be economically designed on-chip (as they increase the test circuitry area which results in additional cost).

In order to decrease the production test cost and to make BIST ADCs practical, it is required to design new test methods that can relax the above stringent conditions to perform accurate ADC spectral test. In this dissertation, three methods are proposed to relax some of the aforementioned challenging conditions for ADC spectral test.

IV. DISSERTATION ORGANIZATION

Three new test methods that address the aforementioned challenges to perform spectral testing are presented in this dissertation. As mentioned earlier, the methods can be applied to test high performance ADCs or high performance waveform generators. These methods can be used either in production testing or in BIST applications to decrease the test cost. The dissertation is arranged in the following order.

In Chapter 2, a method called the Fundamental Identification and Replacement (FIRE) method is presented. With FIRE, the requirement of coherent sampling to perform accurate ADC spectral testing [7-10] is completely eliminated. A new approach to identify the fundamental in a non-coherently sampled data set using frequency domain data and Newtons method is proposed. Though non-coherent, the samples must be uniformly spaced. The validity of the method is shown using measurement data from commercially available high resolution ADCs. The use of this method can decrease the test costs associated with achieving coherent sampling.

In Chapter 3, the Fundamental Estimation, Removal And Residue Interpolation (FERARI) method is presented [11-12]. This method simultaneously relaxes the requirement to have precise control over amplitude and frequency of the input signal in order to test ADCs. A new fundamental estimation technique is proposed that can be used when the ADC output is clipped and is sampled non-coherently with uniform spacing. Measurement results are provided to validate this method using a commercially available 16-bit ADC. The method can be used in BIST applications as precise amplitude and frequency control is costly to achieve in such systems.

In Chapter 4, a method of relaxing the conditions of using a spectrally pure sinusoidal input source and simultaneously removing the requirement of coherent sampling is proposed [13-14]. The sampled points need to be uniformly spaced. The non-linear (impure) input that is non-coherently sampled is first characterized using a "Golden ADC". Later, the same input signal is used to test high resolution ADCs accurately. This method is explained in detail in this chapter. The simulation results

show accurate functionality and robustness of the proposed method. This method can be used to decrease the test cost in production testing, where acquiring a source with high spectral purity and obtaining coherent sampling result in high test costs.

In chapter 5, the work done on Metastability in comparators and ADCs is discussed [15]. A rigorous mathematical definition of metastability is presented. The probability of metastability is analyzed and compared for two comparator architectures, one with a latch and the other with a latch followed by an inverter. The probability of metastability of synchronous SAR ADCs with and without using metastable detection circuit is analyzed and compared. The analysis can be used to decide if a metastable detection circuit is necessary to decrease the probability of metastability in SAR ADCs.

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CHAPTER 2

FIRE: A FUNDAMENTAL IDENTIFICATION AND REPLACEMENT METHOD FOR ACCURATE SPECTRAL TEST WITHOUT REQUIRING COHERENCY

Achieving coherent sampling is one of the major bottlenecks to perform ADC spectral test, especially when high-precision instruments or high-performance frequency synthesizes are not readily available. If coherent sampling is not achieved, there could be huge leakage in the spectrum which might lead to inaccurate test results. In this chapter, a new Fundamental Identification and Replacement method is presented that can completely eliminate the need for coherent sampling in spectral testing. A 2-step Fundamental Identification method is used to very accurately estimate the non-coherent fundamental. Extensive simulation results show the functionality and robustness of the method. Measurement results obtained in industry labs using commercially available high resolution ADCs successfully validate the proposed method for both accuracy and robustness.

I. INTRODUCTION

In chapter 1, it was recommended to achieve coherent sampling to obtain accurate spectral results of an ADC. However, to achieve coherent sampling, it is required to obtain high accuracy frequency synthesizers and Phase Locked Loops (PLL). This results in increase in test cost and test area.

Another case is, during characterization of an ADC, the spectral characteristics of the ADC at various input frequencies need to be tested. It would take more test time to achieve coherent sampling in such cases as the frequencies of input signal and clock signal need to be tuned for each input frequency separately to achieve coherent sampling. This tuning increases the test cost and the product delivery time.

Also looking into the future, there is a strong drive to design circuits that have Built-in Self-Test (BIST) capability to decrease the test cost. The area required by the testing circuitry should be very small compared to that of the Device under Test (DUT). In such circuits, it is impossible to achieve coherent sampling with a self-contained oscillator as signal source implemented on a very small area.

In the above mentioned cases, it is either expensive or more time consuming or impossible to achieve coherent sampling. So, there is a strong need to develop new low cost test methods that can eliminate the condition of coherent sampling and still provide accurate spectral results.

A. State of the art methods for Non-coherent sampling

The state-of the-art methods proposed in the literature to perform accurate spectral test using non-coherently sampled data are discussed below.

1) Windowing technique

Windowing technique is one of the widely used methods to obtain spectral characteristics from a non-coherently sampled data [1-6]. To obtain accurate spectral results with windows, the spectral power of secondary lobes of selected window should

be lower than the noise power of the ADC under test. This requires prior knowledge about the type of window to be used to accurately test the ADC. If a window with power in secondary lobes greater than the noise floor of the ADC under test is used, inaccurate results of spectral parameters are obtained. As a result, the spectral characteristics obtained are window dependent. Also, for large non-coherent sampling and high resolution ADCs, not all windows can achieve accurate spectral results [7].

2) Four parameter Sine Fitting technique

The four parameter sine fitting method is used to characterize analog-to-digital converters and digital oscilloscopes for THD and ENOB [8-11]. In this method, the time domain data is used to identify the four parameters in the non-coherently sampled fundamental, namely, frequency (*f*), amplitude, offset and phase. Since the time domain data is a non-linear function of frequency (*f*), a non-linear method such as Newton method is used to identify the above four parameters. With this, the power of fundamental can be accurately estimated. Now, the identified fundamental is removed from the data to obtain the residue. Later, using the frequency value (*f*) obtained from four parameter sine fitting, a three parameter fit (amplitude, phase, offset) on the residue is performed for each harmonic component (with frequencies 2*f*, 3*f*, …). Once the powers of all harmonics are obtained, the spectral parameters such as THD and SNR can be estimated using equations (1.8).

The four parameter sine fitting method gives accurate values of THD, SNDR and ENOB. Also, when the harmonic component determines SFDR, accurate value of SFDR is obtained. However, when a non-harmonic component determines SFDR as shown in

Fig. 2.1, the method cannot provide accurate value. In such cases, a method intended for full spectrum test is required. Furthermore, computational efficiency is one of the concerns when data record length is large. In [12], a multi-sine fitting algorithm was proposed to accurately estimate the fundamental and harmonics of the signal. However, the method also cannot provide accurate value of SFDR when a non-harmonic component has the highest power (excluding the fundamental) in the spectrum.

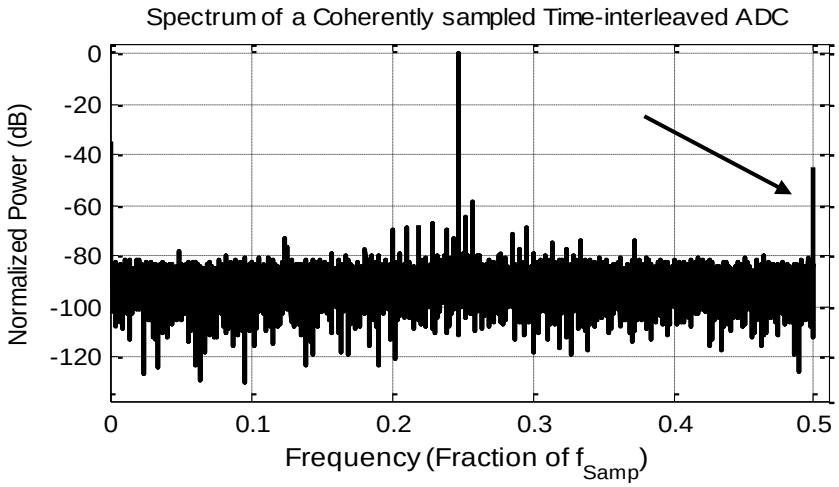

Figure 2.1: Power Spectrum of a coherently sampled time-interleaved ADC showing non-harmonic spur

3) Other state-of the-art methods

In the recent past, several other methods have been proposed to relax the condition of coherency for spectral testing [13]. A 2-D FFT method was introduced in [14] with a time complexity of O ($M^2 \log^2 M$), where M is the total data record length. A singular value decomposition method was proposed in [15] which involve a time complexity of O (M^3). In [16], a filter bank method was reported which results in an increase in testing circuitry area. A resampling technique was presented in [17], which

again results in increasing area due to additional decimator used. In [18-22], interpolating DFT (IpDFT) methods were used to eliminate the requirement of coherency. However, such methods cannot provide accurate value of SFDR when a non-harmonic spur dominates the harmonics. In [23], a fundamental identification and replacement method was proposed that can accurately estimate the spectral characteristics. However, the method is not robust to signal frequencies that are close to Nyquist range.

All the above methods suffer from one or more of the issues such as, large computation time, increase in area, lack of robustness across the Nyquist range, dependency of results on the type of window chosen or the inability to perform full spectrum test. So, it is required to develop a test method that can address all the above issues and accurately perform spectral test without requiring coherent sampling.

In [7], a Fundamental Identification and Replacement method was proposed that is robust over any level of non-coherency. The method provides accurate spectral results for ADCs with medium resolution. However, for very high resolution ADCs, the estimated spectral parameters have errors as the accuracy with which the fundamental was identified was not sufficient.

In this chapter, a new fundamental identification and replacement (FIRE) method that addresses all the above issues and performs accurate spectral testing is presented. Compared to the method in [7], a new 2-step fundamental identification method that can very accurately estimate the fundamental is proposed. The initial estimates of parameters are obtained in Step 1 using closed form expressions. In Step 2, Newton method is used

to accurately estimate all the parameters. The estimation is done using the frequency domain data and is computationally efficient. The estimated non-coherent fundamental is later removed from the initial data to obtain the residue. A fundamental that is coherently sampled is added to the residue and DFT is performed on the final data to obtain accurate spectral results. The functionality and robustness of proposed FIRE method is verified using both simulation and measurement data.

The remainder of the chapter is arranged as follows. The issue of Non-coherent sampling is described in Section II. Section III provides a detailed description of proposed FIRE method. Section IV presents the simulation results and Section V validates the FIRE method using measurement data. Section VI concludes the chapter.

II. ISSUES WITH NON-COHERENT SAMPLING

If the input signal is not coherently sampled, J in equation (1.3) is not an integer and as a result, the spectrum of such output data may contain severe skirting as shown in Fig. 2.2. This phenomenon is widely known as spectral leakage.

From chapter 1, let $x(t)$ in (1.2) be the pure input source to the ADC. If the input is non-coherently sampled by the ADC, the output of ADC can be given by equation (2.1) (similar to equation 1.3) after calibrating gain error and offset. $x[n]$ is the analog representation of the n^{th} sampled digital output of ADC. All the parameters in (2.1) are similar to the parameters defined in chapter 1. $x[n]$ is obtained after considering only the first H harmonics. It is assumed that the higher harmonics have negligible power.

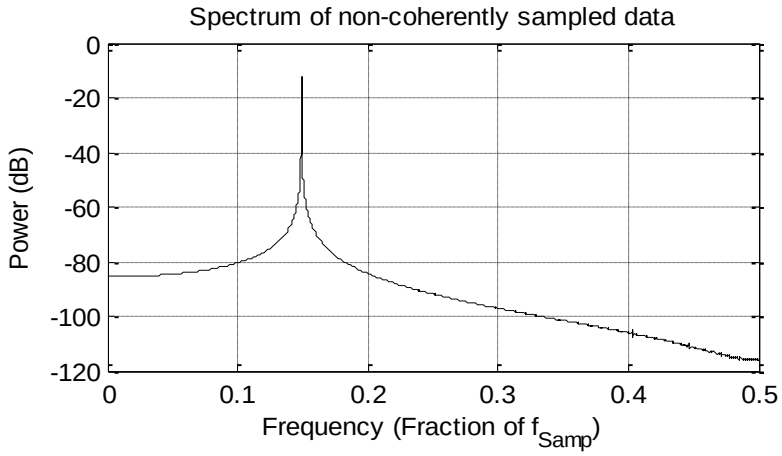

Figure 2.2: Power spectrum of a non-coherently sampled ADC Output

$$x[n] = A\cos\left(\frac{2\pi J}{M}n + \phi\right) + \sum_{h=2}^{H} A_h \cos\left(\frac{2\pi hJ}{M}n + \phi_h\right) + w[n] \tag{2.1}$$

It should be noted that J in (2.1) is no longer an integer. Let $J = J_{int} + \delta$, where J_{int} represents the integer part of J and δ represents the non-integer part of J. δ varies from -0.5 to 0.5. The DFT of non-coherently sampled $x[n]$ in (2.1) can be obtained using equation (2.2). Substituting non-integer J in (2.1) and (2.2), the kth DFT coefficient, X_k, can be given as (2.3).

$$X_k = \frac{1}{M}\sum_{n=0}^{M-1} x[n] e^{-j\frac{2\pi k}{M}n}, \; for \; k = 0,1,2,...,M-1 \tag{2.2}$$

It can be seen that unlike in equation (1.5), the contribution from fundamental and harmonics on to other frequency bins is no longer zero in equation (2.3) due to the presence of non-integer δ. As a result, using equations (1.6-1.8) to test spectral characteristics of a non-coherently sampled data, results in inaccurate values. Such cases

of non-coherent sampling are very common and it is important to design a test method that can perform full spectrum Test in spite of having non-coherent sampling.

$$X_k = \left(\begin{array}{l} \dfrac{A}{2M}\left\{ \dfrac{\sin\left(\pi\left(J_{\text{int}}+\delta-k\right)\right)}{\sin\left(\dfrac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)} e^{j\left(a\left(J_{\text{int}}+\delta-k\right)+\phi\right)} + \dfrac{\sin\left(\pi\left(J_{\text{int}}+\delta+k\right)\right)}{\sin\left(\dfrac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)} e^{-j\left(a\left(J+k\right)+\phi\right)} \right\} \\ +\sum_{h=2}^{H} \dfrac{A_h}{2M}\left\{ \begin{array}{l} \dfrac{\sin\left(\pi\left(hJ_{\text{int}}+h\delta-k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)} e^{j\left(a\left(hJ_{\text{int}}+h\delta-k\right)+\phi_h\right)} \\ + \dfrac{\sin\left(\pi\left(hJ_{\text{int}}+h\delta+k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)} e^{-j\left(a\left(hJ_{\text{int}}+h\delta+k\right)+\phi_h\right)} \end{array} \right\} \end{array} \right) \quad (2.3)$$

III. FUNDAMENTAL IDENTIFICATION AND REPLACEMENT (*FIRE*) METHOD

In this section, a test method is proposed that can take in non-coherently sampled ADC output and perform full spectrum test. Before describing the method in detail, a brief description about the foundation for Fundamental Identification and Replacement methods [7, 23-26] is presented.

It can be said that when DFT is applied on non-coherently sampled data, the leakage in the spectrum is mainly due to the fact that the fundamental component is non-coherently sampled. It can also be stated that for high resolution ADC testing, the leakage from any frequency bin (other than the fundamental) to any other frequency tone

is significantly below the total noise power of the ADC. This effect of non-coherent fundamental is shown in Fig. 2.3 and Fig. 2.4.

Fig. 2.3 is the spectrum of a non-coherently sampled data. As explained earlier, there is severe spectral leakage around the fundamental. However, it can be seen that if the non-coherent fundamental in this data is identified and removed, accurate information of harmonics and noise can be obtained from the spectrum of residue as shown in Fig. 2.4. So, it is required to accurately identify the non-coherent fundamental to obtain correct spectral results.

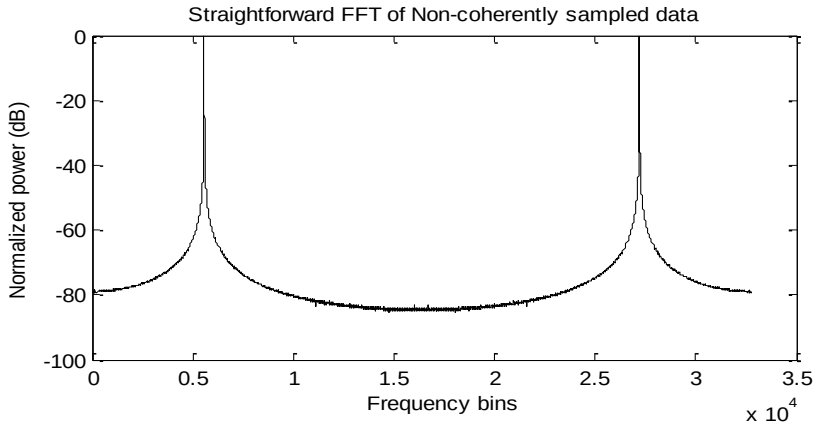

Figure 2.3: Spectrum of FFT of non-coherently sampled data showing leakage

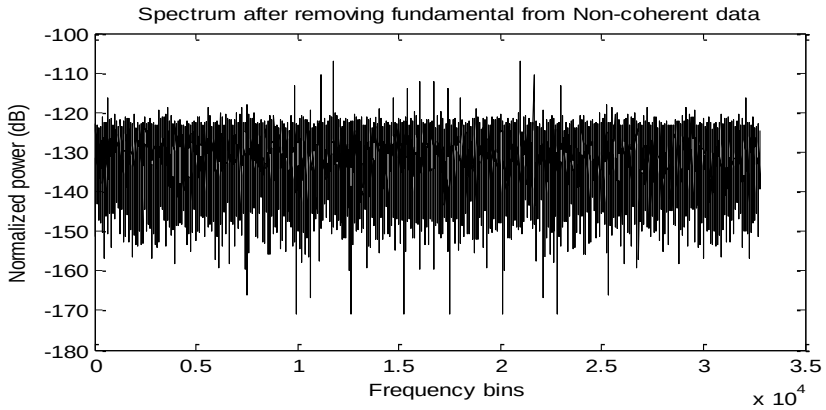

Figure 2.4: Spectrum of residue obtained after removing the fundamental

A) Fundamental Identification

Several methods were presented in the past to identify the fundamental in a non-coherently sampled data [18-22, 27]. One of the proposed methods is the Interpolated Discrete Fourier Transform (IpDFT). The IpDFT methods start from applying windows on the non-coherently sampled data and later perform interpolation to accurately estimate the fundamental component [18-22]. In [22], a criterion to choose the optimal window to obtain accurate spectral characteristics was proposed. However, in the proposed FIRE method, the fundamental is identified from the DFT of non-coherently sampled data without using windows. As a result, the method is not dependent on windows and can accurately estimate the fundamental.

Substituting $J = J_{int} + \delta$ in equation (2.1), in order to identify the fundamental in $x[n]$, it is required to estimate the values of J_{int}, δ, A and ϕ. In the proposed FIRE method, the fundamental component is identified in a two-step process. First step provides the value of J_{int} and initial estimates of δ, A and ϕ from the DFT of non-coherently sampled data. The second step obtains accurate estimates of δ, A and ϕ using Newton method. The procedure to identify the fundamental is explained in detail below.

1) First Step

The time domain output data of the ADC, $x[n]$ in (2.1) is converted to frequency domain data by taking the DFT of $x[n]$ which is given by X_k in equation (2.2). Using DFT coefficients, the value of J_{int} and initial values of δ, A and ϕ are estimated.

a) Estimate J_{int} and δ

J_{int} is estimated by taking the index of frequency bin in half spectrum that contains the maximum power excluding the DC component and is given by (2.4).

$$J_{\text{int}} = \arg\max_{1 \le k \le (M/2)} |X_k| \tag{2.4}$$

The initial value of δ can be estimated with a three-point calibration method using the DFT coefficients. Using (2.3), for $k = J_{int}$, X_k represents the DFT coefficient of the fundamental and for $k = J_{int}+1$ and $J_{int}-1$, X_k represents the DFT coefficients of the adjacent bins on either side of the fundamental bin. For high resolution ADCs, when estimating the fundamental, the effect of harmonics can be neglected. Also, in order to obtain a closed form expression for initial value of δ, the term containing $e^{-j(a(J+k+\delta)+\phi)}$ can be neglected compared to the term containing $e^{j(a(J+k+\delta)+\phi)}$ for $M > 1024$ [28]. The neglected term is later considered in the equations to obtain an accurate estimate of δ in the second step. After neglecting the above mentioned terms, X_k can be given by (2.5).

$$X_k \approx \frac{A}{2M} e^{j\phi} \frac{1 - e^{j2\pi(J-k)}}{1 - e^{j\frac{2\pi(J-k)}{M}}} \tag{2.5}$$

Let $Y = e^{j2\pi\delta}$ (2.6)

For $k = J_{int}$, $J_{int}+1$ and $J_{int}-1$, using (2.5)

$$X_{J_{\text{int}}} = \frac{A}{2M} e^{j\phi} \frac{1 - e^{j2\pi\delta}}{1 - e^{j\frac{2\pi\delta}{M}}} = \frac{A}{2M} e^{j\phi} \frac{1 - Y}{1 - Y^{1/M}} \tag{2.7}$$

$$X_{J_{\text{int}}+1} = \frac{A}{2M} e^{j\phi} \frac{1-e^{j2\pi\delta}}{1-e^{j\frac{2\pi(\delta-1)}{M}}} = \frac{A}{2M} e^{j\phi} \frac{1-Y}{1-Y^{1/M} e^{-j\frac{2\pi}{M}}} \tag{2.8}$$

$$X_{J_{\text{int}}-1} = \frac{A}{2M} e^{j\phi} \frac{1-e^{j2\pi\delta}}{1-e^{j\frac{2\pi(\delta+1)}{M}}} = \frac{A}{2M} e^{j\phi} \frac{1-Y}{1-Y^{1/M} e^{j\frac{2\pi}{M}}} \tag{2.9}$$

The above three equations can be used to solve for Y in terms of X_{Jint}, X_{Jint+1} and X_{Jint-1}.

$$Y^{1/M} = e^{j\frac{2\pi\delta}{M}} = \left(\frac{\frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}+1}} - \frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}-1}}}{\frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}+1}} - \frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}-1}} + e^{j\frac{2\pi}{M}} - e^{-j\frac{2\pi}{M}}} \right) \tag{2.10}$$

From equations 2.6 & 2.10, the initial value of δ, δ_0, can be estimated by (2.11) as

$$\delta_0 = \frac{M}{2\pi} imag \left(\ln \left(\frac{\frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}+1}} - \frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}-1}}}{\frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}+1}} - \frac{X_{J_{\text{int}}}}{X_{J_{\text{int}}-1}} + e^{j\frac{2\pi}{M}} - e^{-j\frac{2\pi}{M}}} \right) \right) \tag{2.11}$$

b) <u>Estimate A and ϕ</u>

Now that J_{int} and δ are estimated, the initial values of A and ϕ can be estimated using (2.7). Taking magnitude of X_{Jint} gives the initial value of A, A_0, as shown in equation (2.12).

$$A_0 = 2M\left|X_{J_{\text{int}}}\right|\left|\frac{1-e^{j\frac{2\pi\delta_0}{M}}}{1-e^{j2\pi\delta_0}}\right| \tag{2.12}$$

The initial value of ϕ, ϕ_0, can be estimated by using A_0 and δ_0 as shown in equation (2.13).

$$\phi_0 = -imag\left(\ln\left(\frac{2MX_{J_{\text{int}}}}{A_0}\frac{1-e^{j\frac{2\pi\delta_0}{M}}}{1-e^{j2\pi\delta_0}}\right)\right) \tag{2.13}$$

Hence, using equations (2.4, 2.11-2.13), J_{int} and the initial values of δ, A and ϕ are estimated.

2) Second Step

It can be noted that equation (2.5) involves an assumption to neglect $e^{-j\left(a\left(J_{\text{int}}+k+\delta\right)+\phi\right)}$ term. The error in estimating the value of δ for 1000 runs using this assumption is as shown in Fig. 2.5. It can be seen that the values of 1000 randomly selected δ's were estimated with a maximum error of about 10^{-4}. However, to perform high resolution ADC test, the estimation error should be very small. Also, in order to propose a method that is independent of the resolution of ADC, the error should only be limited by the noise power per bin (i.e., P_{noise}/M). To obtain these requirements, it is necessary to include $e^{-j\left(a\left(J_{\text{int}}+k+\delta\right)+\phi\right)}$ term in estimating the three parameters δ, A and ϕ. The expression of X_{Jint} without neglecting $e^{-j\left(a\left(J_{\text{int}}+k+\delta\right)+\phi\right)}$ term is as shown below in (2.14). It can be shown that the expression is a non-linear equation in δ. Also, X_{Jint} can

be represented with both real and imaginary parts given by R_{Jint} and I_{Jint} respectively as shown in (2.15). It should be noted that both R_{Jint} and I_{Jint} are functions of J_{int}, A, δ and ϕ.

$$X_{J_{\text{int}}} = \frac{A}{2M} e^{j\phi} \frac{1-e^{j2\pi\delta}}{1-e^{j\frac{2\pi\delta}{M}}} + \frac{A}{2M} e^{-j\phi} \frac{1-e^{-j2\pi(2J_{\text{int}}+\delta)}}{1-e^{-j\frac{2\pi(2J_{\text{int}}+\delta)}{M}}} \tag{2.14}$$

$$X_{J_{\text{int}}} = R_{J_{\text{int}}}\left(J_{\text{int}}, A, \delta, \phi\right) + jI_{J_{\text{int}}}\left(J_{\text{int}}, A, \delta, \phi\right) \tag{2.15}$$

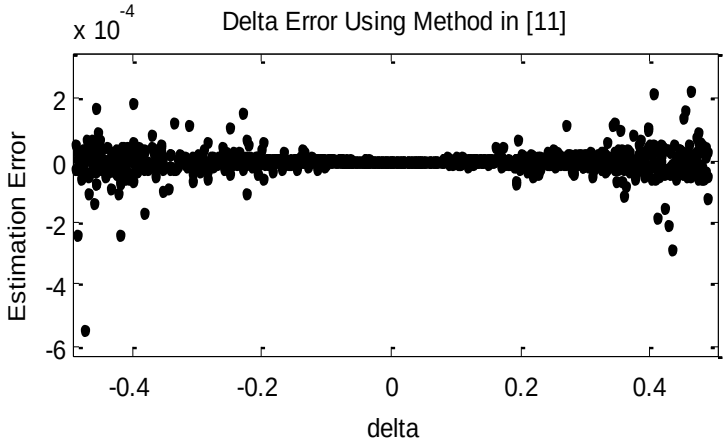

Figure 2.5: Error in estimating δ versus actual value of δ using equation (2.11).

Similarly, X_{Jint+1} and X_{Jint-1} need to be modified from (2.8-2.9) to include the neglected term in (2.5). It can be seen that two equations are obtained by taking the real part and imaginary part of (2.15) separately. Doing the same for X_{Jint+1} and X_{Jint-1}, a total of six equations are obtained. Let the six equations be given as $f_1,..,f_6$. (2.16-2.21).

$$f_1\left(J_{\text{int}}, A, \delta, \phi\right) = R_{J_{\text{int}}}\left(J_{\text{int}}, A, \delta, \phi\right) - real\left(X_{J_{\text{int}}}\right) \tag{2.16}$$

$$f_2\left(J_{\text{int}}, A, \delta, \phi\right) = I_{J_{\text{int}}}\left(J_{\text{int}}, A, \delta, \phi\right) - imag\left(X_{J_{\text{int}}}\right) \tag{2.17}$$

$$f_3\left(J_{\text{int}}, A, \delta, \phi\right) = R_{J_{\text{int}}+1}\left(J_{\text{int}}, A, \delta, \phi\right) - real\left(X_{J_{\text{int}}+1}\right) \tag{2.18}$$

$$f_4\left(J_{\text{int}}, A, \delta, \phi\right) = I_{J_{\text{int}}+1}\left(J_{\text{int}}, A, \delta, \phi\right) - imag\left(X_{J_{\text{int}}+1}\right) \tag{2.19}$$

$$f_5\left(J_{\text{int}}, A, \delta, \phi\right) = R_{J_{\text{int}}-1}\left(J_{\text{int}}, A, \delta, \phi\right) - real\left(X_{J_{\text{int}}-1}\right) \tag{2.20}$$

$$f_6\left(J_{\text{int}}, A, \delta, \phi\right) = I_{J_{\text{int}}-1}\left(J_{\text{int}}, A, \delta, \phi\right) - real\left(X_{J_{\text{int}}-1}\right) \tag{2.21}$$

From above six non-linear equations, the three parameters are accurately estimated by Newton method and least squares. Using Newton method, the value of y in $(k+1)^{th}$ iteration, y_{k+1}, is given by equation (2.22).

$$y_{k+1} = y_k - B_k \backslash F_k, \tag{2.22}$$

where "\" operator is the least squares operator, y_k is the vector containing the 3 estimated parameters in k^{th} iteration, F_k is the vector of $f_1..f_6$ evaluated using estimated values in y_k and B_k is the Jacobean matrix evaluated using values in y_k as shown below.

$$B_k = \begin{bmatrix} \frac{\partial f_1}{\partial A} & \frac{\partial f_1}{\partial \delta} & \frac{\partial f_1}{\partial \phi} \\ \cdot & \cdot & \cdot \\ \cdot & & \\ \cdot & & \\ \cdot & & \\ \frac{\partial f_6}{\partial A} & \frac{\partial f_6}{\partial \delta} & \frac{\partial f_6}{\partial \phi} \end{bmatrix}_{y_k} \quad F_k = \begin{bmatrix} f_1 \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ f_6 \end{bmatrix}_{y_k} \quad y_k = \begin{bmatrix} A \\ \delta \\ \phi \end{bmatrix}_k \tag{2.23}$$

It can be mentioned that this method always converges to a global minima as the initial points to start the iterations are very close to the actual values. Also, it can be

noticed that the number of operations in each iteration is no longer dependent on the length of the data record. Each iteration involves 6 equations and 3 unknowns, thus making the method more computationally efficient compared to other sine fitting methods [9-12] that use total data record for each iteration. Using rigorous simulation study, it is seen that a maximum of 5 iterations would always result in delivering precise values of the 3 parameters, thus, accurately estimating the fundamental. This accuracy in estimating the three parameters is limited by the noise power per bin (Fig. 2.7). The error in estimating the same 1000 values of δ's (as in Fig. 2.5) using this 2-step method is shown in Fig. 2.6. It can be seen that, the estimation error using the 2-step method is decreased by three orders (from 10^{-4} to 10^{-7}) compared to that using equation (2.11). Also the error obtained using this method is only limited by the noise power per bin as shown in Fig. 2.7. A total of 50 randomly selected values of δ for each value of SNR are considered and the error in estimating δ is noted down. The data record length (M) for all runs is 4096. With constant data record length (M) and signal power, as the value of SNR increases, the noise power per bin decreases. It can be seen from Fig. 2.7 that, as the noise power per bin decreases (i.e., as SNR increases), the estimation error also decreases and more accurate values of δ can be obtained. Hence, the proposed 2-step fundamental identification method accurately estimates the fundamental component and the accuracy is only limited by the noise power per bin. Let the final estimates of δ, A and ϕ be given as $\hat{\delta}$, $\hat{A}$ and $\hat{\phi}$ respectively.

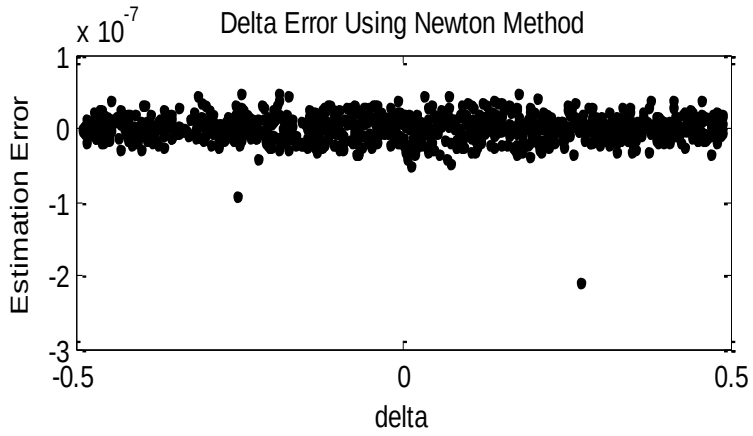

Figure 2.6: Error in estimating δ versus actual value of δ using 2-step method

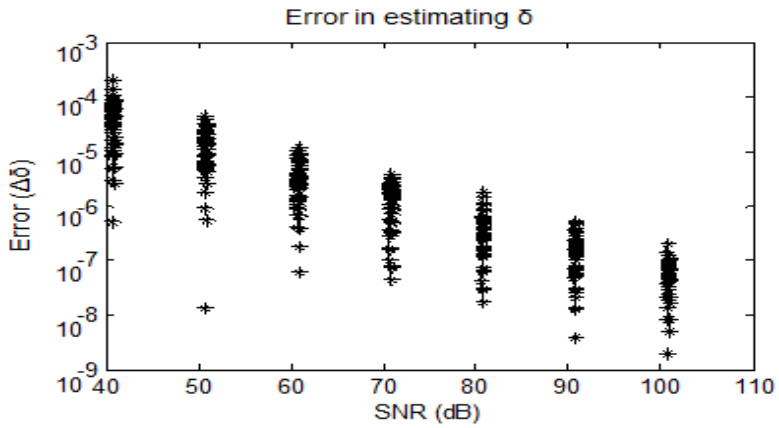

Figure 2.7: Error in estimating δ using 2-step method for different SNR values. With fixed signal power, as SNR increases, estimation error decreases

B) Estimate the non-coherent fundamental

Using $\hat{\delta}$, $\hat{A}$ and $\hat{\phi}$, the non-coherent fundamental component in *x[n]* can be estimated as *x_nc[n]* and is given as

$$x\_nc[n] = A\cos\left(\frac{2\pi\left(J_{\text{int}}+\delta\right)}{M}n+\hat{\phi}\right) \tag{2.24}$$

C) Construct a coherent fundamental

The fundamental component that is coherent (signal corresponding to J_{int} cycles) can be constructed using $\hat{A}$ and $\hat{\phi}$, and is given as *x_c[n]* as shown in (2.25).

$$x\_c[n] = A\cos\left(\frac{2\pi J_{\text{int}}}{M} n + \hat{\phi}\right) \tag{2.25}$$

D) Fundamental Replacement

Using equations (2.24) and (2.25), the non-coherent fundamental can be removed from the output of ADC and replaced by a coherent fundamental. This replaced output is given as $x_{new}[n]$ in equation (2.26).

$$x_{new}[n] = x[n] - x\_nc[n] + x\_c[n] \tag{2.26}$$

Since the non-coherent fundamental component in *x[n]* is replaced with a coherent fundamental in $x_{new}[n]$, taking FFT of $x_{new}[n]$ gives accurate spectral results (SNR, SFDR, THD). Thus, the method can be used to perform full spectrum test without using windows and without large increase in area and test time (as shown in Simulation results).

The flow chart in Fig. 2.8 summarizes the steps to be performed for spectral test using FIRE Method.

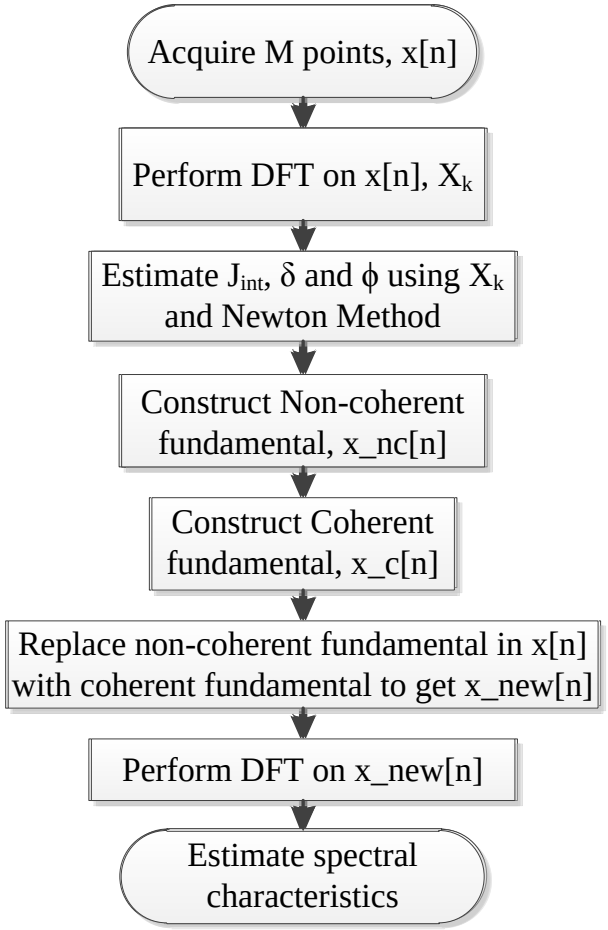

Figure 2.8: Flow Chart to perform spectral testing using proposed FIRE method

IV. SIMULATION RESULS

In this section, simulation results to verify the functionality and robustness of the proposed FIRE method are presented. The computation time of the proposed method is also compared along with other methods used for non-coherent sampling. In Section IV and Section V, one data stream was used to estimate the spectral characteristics. The data record length was selected to accommodate the effect of noise.

A) Functionality

An 18-bit ADC was generated using MATLAB with an INL of 1.2 LSB. The true THD, SFDR and SNR values of the ADC are obtained by sending a pure sine wave that is coherently sampled. Later, a non-coherently sampled pure sine wave with same amplitude is sent to the same ADC and the proposed method is used to obtain spectral characteristics.

Fig. 2.9 shows three spectrums of the same ADC obtained using the following cases. The Blue spectrum is obtained when the ADC is coherently sampled with M = 16384 and J = 593.00. The spectrum is clean without any leakage. The other two spectrums are obtained using non-coherently sampled data with J = 593.1237. The Green spectrum is obtained when DFT is directly performed on the non-coherently sampled data. As expected, there is severe leakage in the spectrum due to non-coherency (δ = 0.1237). However, using proposed FIRE method on the same non-coherently sampled data, the leakage is completely eliminated as shown in the Red spectrum. It can also be seen that the red spectrum exactly matches with the Blue spectrum. Table 2.1 lists the spectral results estimated using the proposed method on non-coherently sampled data and the coherently sampled method. It can be seen that the results obtained from non-coherently sampled data using FIRE method are very close to those obtained using coherent sampling method. This shows that the proposed method accurately estimates the spectral characteristics even when an input signal is not coherently sampled.

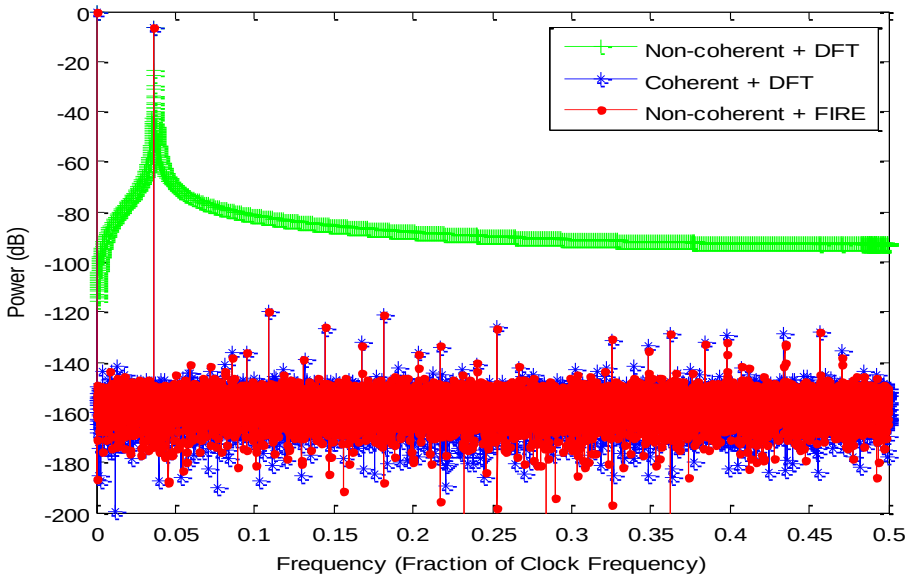

Figure 2.9: Plot showing the spectrum of an ADC for three cases. Blue spectrum is obtained using Coherent sampling (J_{int} = 593), Red spectrum is obtained using the proposed FIRE method on non-coherently sampled data (J = 593.1237) and Green spectrum is obtained after performing DFT on the same non-coherently sampled data.

TABLE 2.1: Spectral Results of 18-bit ADC corresponding to Fig. 2.9

Method	**THD (dB)**	**SFDR (dB)**	**SNR (dB)**
Coherent + DFT (Ideal)	-110	113.7	108.5
Non-coherent + FIRE	-109.7	113.6	108.6

B) Robustness

The robustness of the method with signal frequency and non-coherency is also presented. An 18-bit ADC with INL of 2.4 LSB was simulated. 1000 values of δ and J_{int} corresponding to input signal are randomly generated. The values of δ and J_{int} range from -0.5 to 0.5 (the whole range of δ) and from 0 to $M/2$ (whole Nyquist range)

respectively. The THD, SFDR and SNR of the ADC obtained by coherent sampling are -104.2dB, 107.5dB and 108dB respectively. The errors obtained in estimating the THD, SFDR and SNR values of the ADC with respect to signal frequency (given as a fraction of sampling frequency) are shown in Fig. 2.10. It can be seen that the values are very accurately estimated and the method is robust for input signal frequency in the whole Nyquist range. Fig. 2.11 shows the errors in THD, SFDR and SNR with respect to non-coherency, δ. The errors are attributed due to several factors such as noise, the accuracy with which the parameters are estimated and also the change in spectral parameters due to slight change in frequency (as changing δ changes the input frequency). It can also be seen that the method is robust over the whole range of δ, from -0.5 to 0.5. Hence, the method is robust for input signal frequencies in the whole Nyquist range and for any non-coherency.

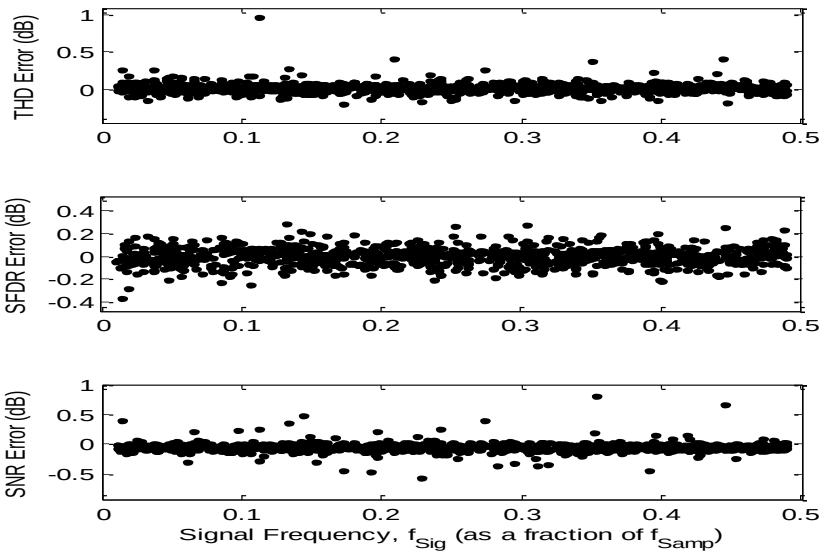

Figure 2.10: Error in estimating THD, SFDR and SNR over the whole range of input signal frequency (From DC to Nyquist range)

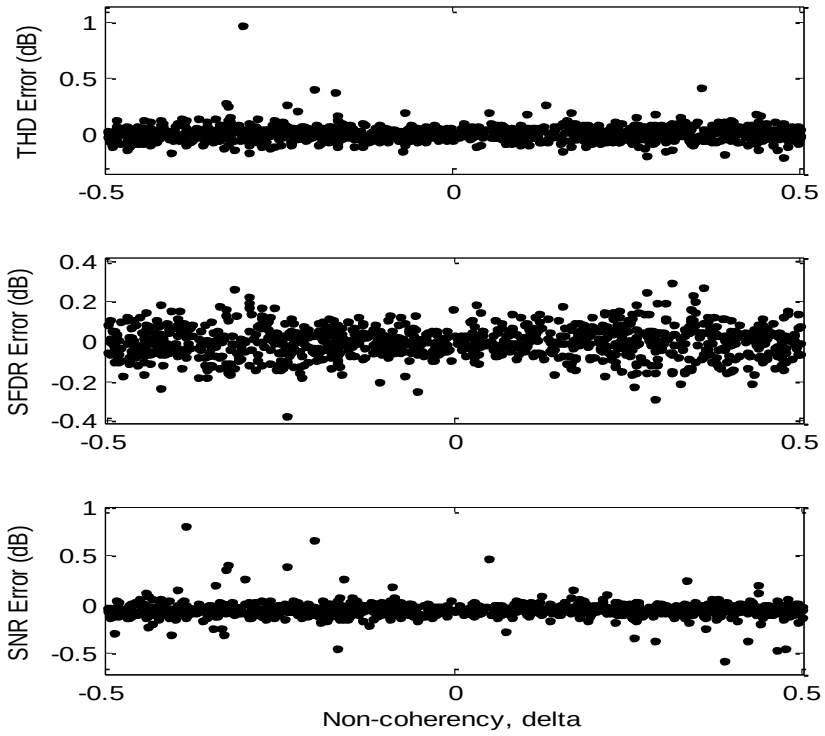

Figure 2.11: Error in estimating THD, SFDR and SNR over the whole range of non-coherency in the fundamental, δ (From -0.5 to 0.5)

C) Computation Time

The calculation time complexity of the proposed method is of the order of $M*\log_2 M$, since, performing FFT is the only major time consuming block. The time taken by the proposed FIRE method is compared with different windows, the best data record length method [23] and a Four parameter sine fitting method [8] in Table 2.2 (using MATLAB on a 64-bit, Intel Core i5 CPU with 4GB memory). It can be seen that of all the methods listed, the proposed method provides accurate test results with least computation time. The method in [23] consumes more time as the best data record length

is not necessarily a power of 2. This results in larger computation time for the FFT algorithm in [23]. It can also be seen from the table that only one window can accurately test an 18-bit ADC while the other three windows cannot be used to test. This shows the dependency of results on the type of window used. As a result, prior knowledge about the resolution of ADC is required to perform spectral test using windows. The computation time using a Four-parameter sine-wave fitting method using time domain data and nonlinear least squares method is shown. Though the method provides accurate estimates of fundamental, it can be seen that using all time-domain data consumes large computation time. As a result, the proposed FIRE method can be readily used to test any resolution ADC to obtain fast and accurate spectral results.

TABLE 2.2: Comparison of Calculation Time (J=519.379, M = 8192, 18-bit ADC, INL = 1.4LSB)

Method	**Time**	**Functionality**
Proposed Method	1.7 ms	Accurate
Best Data Record Method [23]	27.8 ms	Accurate
Window 2 in [29]	2.9 ms	Accurate
Blackman Harris (4-term)	0.7 ms	Inaccurate
Hanning	0.5 ms	Inaccurate
Hamming	0.9 ms	Inaccurate
* Four Parameter Sine Fit (Nonlinear Least Squares)	>25.2 ms	Occasional Inaccurate SFDR

*: Time taken to only estimate the fundamental accurately. Later, 3-parameter fit is required to estimate each harmonic using the total 8192 points which results in more computation time (Clause 8.8.1.3 of [8]).

V. MEASUREMENT RESULTS

In this section, measurement data is used to validate the effectiveness of the proposed FIRE method. Two commercially available ADCs are tested for spectral characteristics with non-coherent sampling using the FIRE method. The first ADC is ADS1282 which is a very high resolution delta-sigma ADC with an SNR of 120dB. This ADC is used to verify the functionality of FIRE method for very high resolution ADCs. The second ADC is ADS8318 which is a 16-bit, 500 kSPS Successive Approximation Register (SAR) ADC. This ADC is used to verify the robustness of proposed FIRE method with respect to whole range of non-coherency, δ, using measurement data.

A) ADS1282 Test (Functionality)

Fig.2.12 shows the test setup used to test ADS1282. DAC1282 is used to provide the pure input signal to test ADC. Both the DAC and ADC are controlled by the same master clock. The ADC sampling clock frequency is 1 kHz and the input signal frequency for coherent sampling is 31.25 Hz. A total of 4096 points were sampled (M). The value of J obtained is 128 for coherent sampling. With this setup, a clean spectrum is obtained and is given by the blue plot in Fig. 2.13. Later, the same ADC is non-coherently sampled with signal frequency given by 30.952 Hz, which results in J equal to 126.781. This corresponds to non-coherent sampling with δ=-0.219. The spectrum of the output of ADC when FFT is applied on this data is given by the green plot in Fig. 2.13. As expected there is severe spectral leakage. However, using the proposed FIRE method on this non-coherently sampled data resulted in a clean and accurate spectrum as shown by the Red plot in Fig. 2.13. It can be seen that the Red spectrum (FIRE) matches

with the Blue spectrum (Coherent) and provides accurate spectral results for a very high resolution ADC. To show the effect of windows on spectral testing, the spectrum obtained when a 4-term Blackman Harris window is used on the same non-coherently sampled data is shown by the purple plot in Fig. 2.13. Blackman Harris window is used here as it is one of the most widely used windows for testing. Table 2.3 compares the values of THD, SFDR and SNR of the ADC using the FIRE method and windows method with the values obtained using Coherent sampling method. It can be seen that the FIRE method accurately estimates the parameters. From the purple plot in Fig. 2.13 and from Table 2.3, it can be said that 4-term Blackman Harris window cannot be used for testing this high resolution ADC. Hence, as mentioned earlier, the choice of window used is dependent on the resolution of ADC.

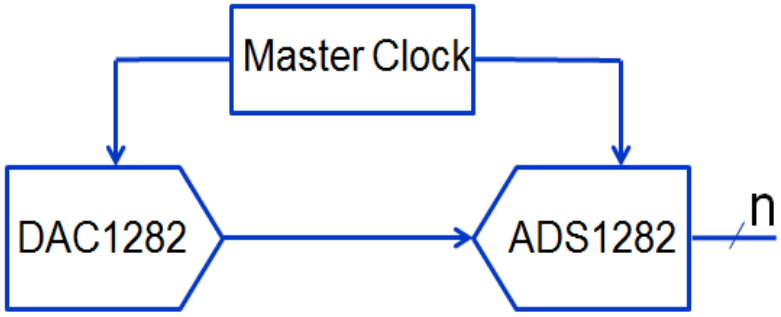

Figure 2.12: Test setup for ADS1282 (f_{Samp} = 1 kHz, M = 4096, $J_{coherent}$ = 128, $J_{noncoherent}$ = 126.781)

TABLE 2.3: SPECTRAL CHARACTERISTICS OF ADS1282 MEASURED USING COHERENT AND NON-COHERENT SAMPLING (IN dB)

METHOD	**THD**	**SFDR**	**SNR**
Coherent	-130.9	133.4	120.3
Non-coherent + FIRE	-129.6	132.3	120.1
Non-coherent + 4-term B-H Window	-126.5	130.8	90.5

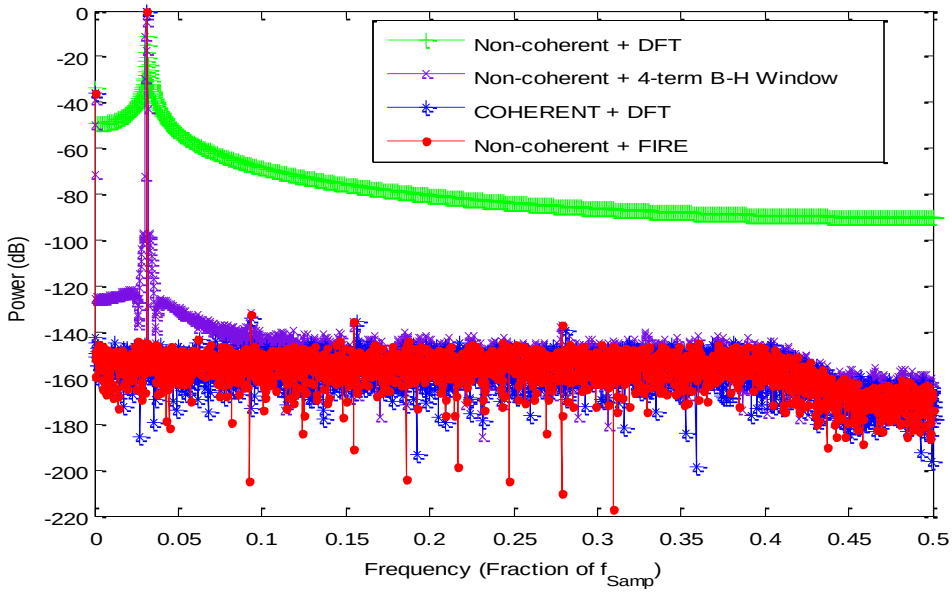

Figure 2.13: Plot showing Spectrum of ADS1282 for 4 different cases. The Blue spectrum is obtained with coherent sampling (J = 128). The Red spectrum is obtained when FIRE method is used on non-coherently sampled data (J = 126.781). The Green spectrum is obtained when DFT is performed on non-coherently sampled data. The purple spectrum is obtained when a 4-term Blackman-Harris (B-H) window is used on the non-coherently sampled data.

B) ADS8318 Test (Functionality and Robustness)

The second ADC that is tested is ADS8318. The test setup is as shown in Fig. 2.14. A signal generator is followed by two band pass filters with center frequency at 10 kHz. The output of the filter is fed to the input of ADC. The ADC is clocked at 500 kSPS and a total of 2048 samples were collected. The input signal frequency to achieve coherent sampling is given by 10.009765625 kHz which gives a value of J equal to 41. Fig. 2.15 shows the values of THD, SFDR and SNR along with the spectrum of ADS8318 with coherent sampling. For a value of δ = 0.46, Fig. 2.16 shows the spectrum of the same ADC using FIRE method. It can again be seen that there is no leakage in the

spectrum in spite of non-coherent sampling and the spectral parameters are very accurately estimated.

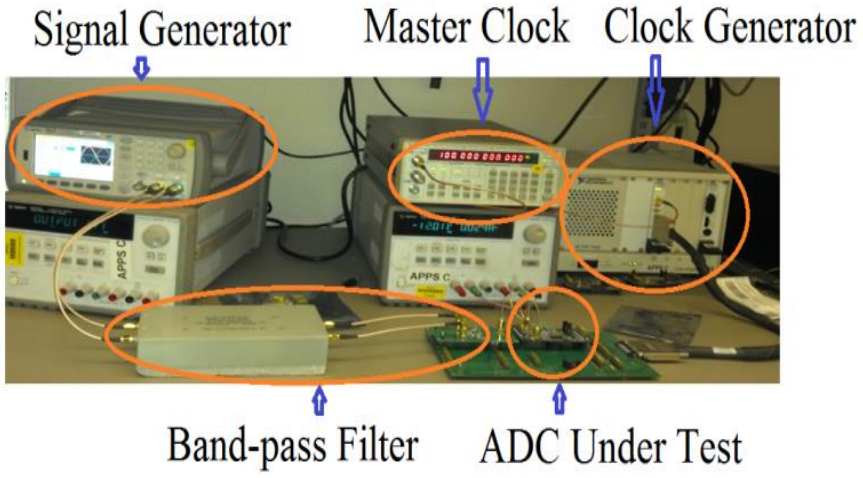

Figure 2.14: Test Setup for ADS8318

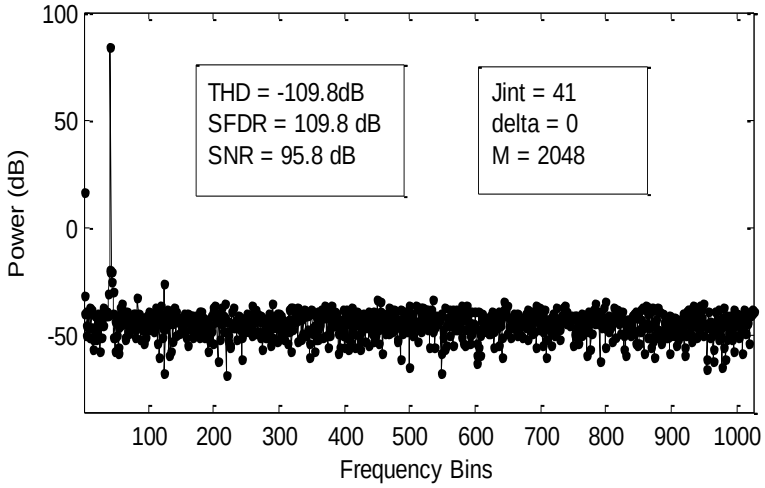

Figure 2.15: Spectrum of ADS8318 using Coherent Sampling

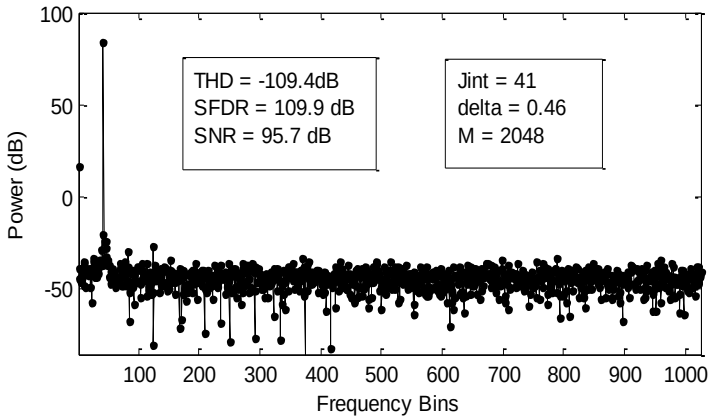

Figure 2.16: Spectrum of ADS8318 using Non-coherent sampling and Proposed FIRE method

Later, to test for robustness of the FIRE method for any value of non-coherency (δ) using measurement data, the frequency of input signal is changed from 9.887 kHz to 10.132 kHz so that the value of J varies from 40.5 to 41.5. This covers the whole range of δ from -0.5 to 0.5. The values of THD, SFDR and SNR are evaluated for each case and plotted in Fig. 2.17, Fig. 2.18 and Fig. 2.19 respectively. The variation of THD, SFDR and SNR for different values of δ is expected as only 2048 points are sampled to test a 16 bit ADC. It can be seen that the values of THD, SFDR and SNR are very accurately estimated using the proposed FIRE method for any value of non-coherency, δ.

Hence, the functionality and robustness of the proposed FIRE method with non-coherent sampling is successfully validated using measurement data from two high resolution ADCs.

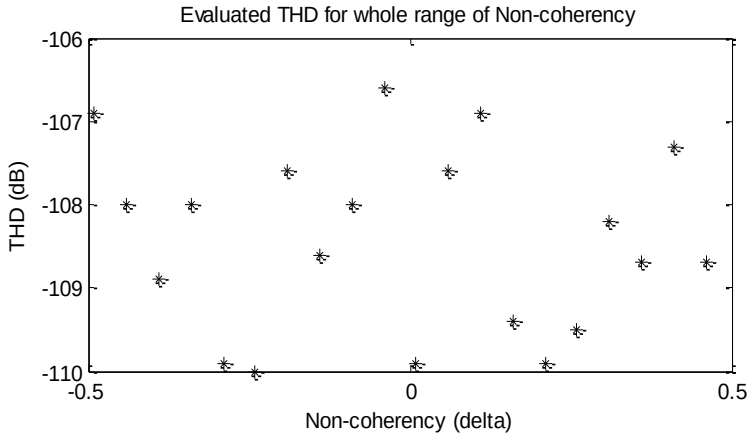

Figure 2.17: Measured THD values over whole range of δ for ADS8318

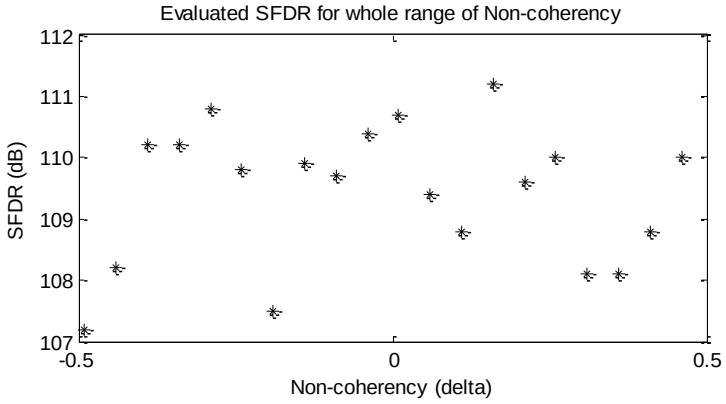

Figure 2.18: Measured SFDR values over whole range of δ for ADS8318

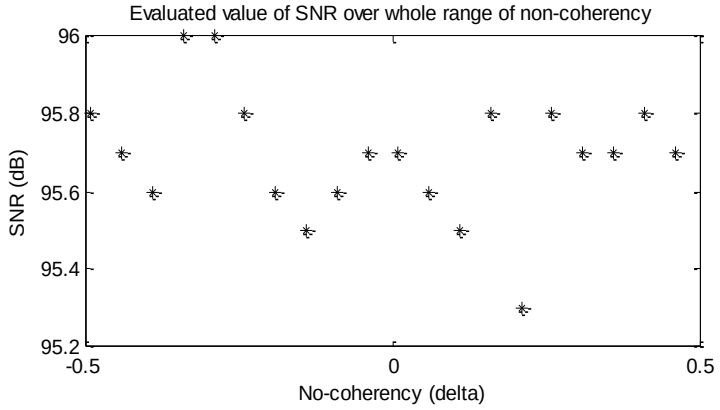

Figure 2.19: Measured SNR values over whole range of δ for ADS8318

VI. CONCLUSION

A new Fundamental Identification and Replacement (FIRE) test method was proposed that completely eliminates the requirement of coherent sampling for full spectrum test. A two-step method using DFT and Newton method was described to accurately identify the non-coherent fundamental. It was shown that the accuracy with which the fundamental was identified is only limited by the noise power per bin (P_{noise}/M). As a result, the method can be readily used to test any ADC output without prior knowledge about the resolution of ADC, unlike windowing method. Simulation results were presented to show the functionality and robustness of the proposed FIRE method with respect to any non-coherency (δ) and to any input signal frequency in the whole Nyquist range. The time complexity of the method is of the order of $M*\log_2(M)$. Thus, all the issues related to previous state of-the art techniques such as, large computation time, large area, lack of robustness of the method over the whole Nyquist range, dependency of the results on the window chosen and inability to perform full spectrum test, have been addressed in the proposed FIRE method. Furthermore, measurement results using two commercially available high resolution ADCs were presented that validated the accurate functionality and robustness of the FIRE method. Finally, it can be said that the FIRE method can be used in all forms of test such as Bench characterization, Final test and BIST, to save the cost and effort associated with achieving coherent sampling.

VII. ACKNOWLEDGMENTS

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CHAPTER 3

FERARI: AN ACCURATE FULL SPECTRUM TEST METHOD ROBUST TO SIMULTANEOUS NON-COHERENT SAMPLING AND AMPLITUDE CLIPPING

For spectral testing of Built-in Self-Test Analog to Digital Converters, it is a very challenging task to precisely control the amplitude and frequency of input sinusoid signal. Amplitude over-range results in clipping ADC output and non-coherent sampling results in spectral leakage. In this chapter, a new method is proposed that provides accurate spectral results even when the input to ADC is both over-ranged and non-coherently sampled. This relaxes the condition to have precise control over the input signal and thus decreases the test cost. The method includes Fundamental Estimation, Removal And Residue Interpolation (FERARI) to obtain accurate spectral results. Simulations show the functionality and robustness of proposed method with both non-coherency and amplitude over-range. Measurement results of a commercially available 16-bit SAR ADC are used to verify the method for both functionality and robustness.

I. INTRODUCTION

In BIST ADCs, since both the testing circuitry and the ADC are present on the same chip, it would be challenging to achieve precise control over frequency and amplitude of the test input sinusoid signal. Due to imprecise frequency control, coherent sampling cannot be achieved unless a master clock is used. However, using master clock on-chip is not an attractive solution as it increases the silicon area. On the other hand,

due to imprecise amplitude control, there could be cases when the input signal to ADC exceeds the input range of ADC. Such cases result in clipped ADC output. Both these situations could occur in BIST ADCs and can result in grossly wrong spectral results if Discrete Fourier Transform (DFT) is performed on such data. As a result, it is important to design a robust method that can accurately test the dynamic characteristics of an ADC even when the input signal is slightly over-ranged and is non-coherently sampled.

In the literature, several methods have been proposed to obtain accurate spectral results when the input is non-coherently sampled. Such methods include windowing method [1-5], interpolating DFT method [6], singular value decomposition method [7], four parameter sine fitting method [8] and fundamental identification and replacement methods [9-11]. However, in the presence of clipped ADC output, none of the above methods provide accurate spectral results.

The issue of over-ranged input was discussed in the recent past. In [12], a method to identify the fundamental and estimate ENOB when the input is over-ranged was proposed. However, the method cannot be used for high resolution ADCs and also cannot estimate all spectral parameters accurately. In [13], a technique to suppress the spurious noises generated by ADC clipping using interpolation of clipped samples was proposed. The method involves oversampling, polynomial spline interpolation and sinc function interpolation which is complex. In [14], oversampling ADC output was used followed by polyphase decomposition to compensate for clipping.

It can be said that none of the methods mentioned above can accurately test spectral characteristics of high resolution ADCs when the input is simultaneously over-

ranged and non-coherently sampled. For BIST ADCs to be practical, it is important to develop such a method. There are two added advantages by developing such a method. The first one is the ability to test the whole input range of ADC and the second one is the ability to use a single method to test both the static and dynamic specifications of an ADC at a given frequency (since static testing usually involves clipping).

In this chapter, such a method that can accurately test the spectral characteristics of ADC when the input signal is slightly over-ranged and is not coherently sampled is proposed. The input over-range is limited to 2% of the input range of ADC. This is a valid and practical limit for BIST ADCs as amplitude of the on-chip input signal to ADC can be controlled up to 2% without any challenges. The proposed method involves accurate estimation of the fundamental component and later subtracts the estimated fundamental from the output of ADC to obtain the residue. The residue is then interpolated to obtain accurate information of ADC's harmonics. The method is called FERARI (Fundamental Estimation, Removal And Residue Interpolation).

The remainder of the chapter is presented as follows. In section II, a brief overview of non-coherent sampling and ADC output clipping is presented. In Section III, a new method (FERARI) is proposed that can accurately estimate spectral characteristics when the ADC output is both clipped and non-coherently sampled. In Section IV, simulations are presented that show the accuracy and robustness of the proposed method. In Section V, measurement results are shown to validate the functionality and robustness of proposed method and Section VI concludes the chapter.

II. EFFECT OF NON-COHERENT SAMPLING AND ADC CLIPPING

Before discussing about the effects of non-coherent sampling and ADC clipping, a brief overview about the ADC input range is presented. For a given N-bit ADC with a gain of 1 and no offset, let T (0 to V_{ADC}) be the total input range of the ADC that covers all the codes from 0 (000...0) to 2^N-1 (111...1) as shown in Fig. 3.1. For any input below 0, the output is clipped at 0(000...0) and for any input above V_{ADC}, the output is clipped at 2^N-1 (111...1). The linear range of the ADC is the range in which the ADC is tested and is recommended to be operated. In major applications, the total range of ADC is tested. In such cases, T would be the linear range. However, in some applications, ADCs are tested only for a partial range in which they are intended to be applied. As shown in Fig. 3.1, the linear range of the ADC that needs to be tested is given by TL (= F_t – F_b), where F_t and F_b are the top and bottom values of range TL respectively. In such cases, if the input is below F_b (above 0) or above F_t (below V_{ADC}), the ADC provides a valid code and does not clip. Taking spectrum of such output would result in pessimistic results as the tested results do not correspond to the actual linear input range. From this point, in this chapter, the term "input range of ADC" corresponds to the linear input range of the ADC that is tested. If T is the input range of ADC that is to be tested, then, F_t =2^N-1 and F_b=0.

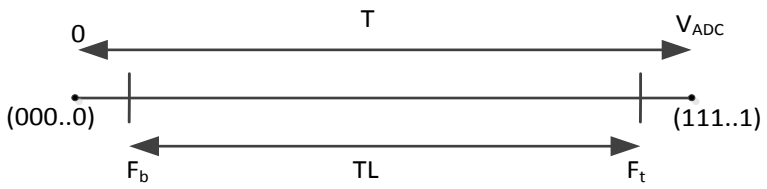

Figure 3.1: Figure showing the total range, T (Codes 000…0 to 111..1) and the linear input range, TL (F_t to F_b) of ADC. T = TL if, F_t = 111..1 and F_b = 000..0.

Let f_{Sig} be the frequency of input signal to ADC, f_{Samp} be the clock frequency, M be the total number of data points recorded to measure the spectral characteristics and J be the total number of periods of the input signal sampled in M points. The four parameters are related by equation (3.1).

$$J = M \frac{f_{Sig}}{f_{Samp}} \tag{3.1}$$

The M point data record is said to be coherently sampled if J in (3.1) is an integer and, non-coherently sampled if J is not an integer.

Let the input range of ADC under test be [F_b F_t] as shown in Fig. 3.1. Let $X(t)$ be the time domain representation of analog input to ADC at time t. $\boldsymbol{X}$ is ideally a pure sine wave without any harmonics and is given by (3.2).

$$X(t) = V_{OS} + A\cos\left(2\pi f_{Sig} t\right) + w(t) \tag{3.2}$$

where, A is the amplitude of fundamental, V_{os} is the DC level and $w(t)$ is the noise at time t. The conditions to obtain in-range and over-range input signals are given by equations (3.3) and (3.4) respectively.

$$(V_{OS} + A <= F_t) \; AND \; (V_{OS} - A >= F_b) \tag{3.3}$$

$$(V_{OS} + A > F_t) \quad OR \quad (V_{OS} - A < F_b) \tag{3.4}$$

It can be mentioned that for standard ADC spectral test, equation (3.3) is satisfied and J in (3.1) is an integer. The procedure to perform standard spectral test was described in chapter 1.

In this section, the issues with simultaneous non-coherent sampling and clipped ADC output are described.

A) Non-coherent Sampling

If the input signal is within the input range of ADC and is not coherently sampled, *J* in (3.1) is not an integer and equation (3.3) is true. The effects of non-coherent sampling alone were discussed in chapter 2. For convenience, the spectrum of a non-coherently sampled, unclipped ADC output data is shown in Fig. 3.2. Severe leakage in the spectrum is observed due to non-coherent sampling.

B) ADC Clipping

If the input signal is coherently sampled and is over-ranged (J in (3.1) is an integer and equation (3.4) is true), the output of ADC is clipped. The spectrum of such clipped data is shown in Fig. 3.3. It can be seen that severe distortion is introduced due to clipping which provides inaccurate spectral results.

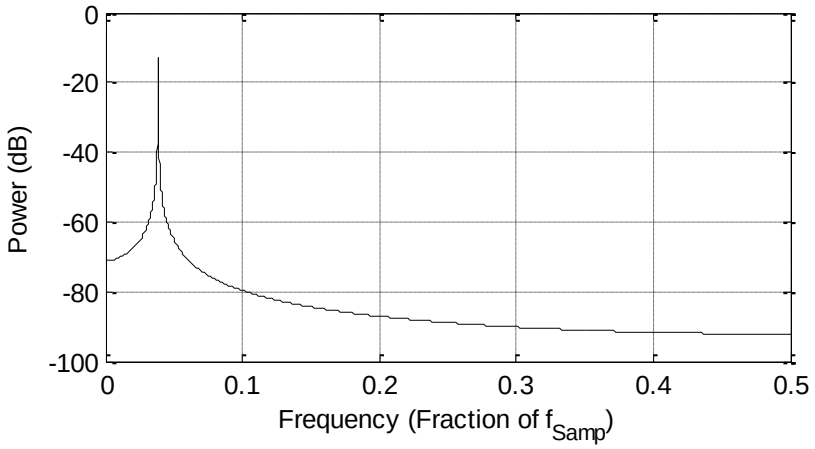

Figure 3.2: Spectrum of a non-coherently sampled, unclipped ADC output data

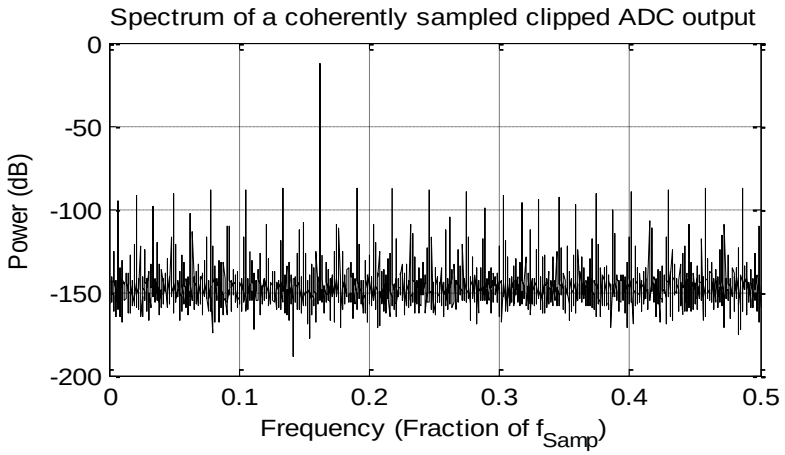

Figure 3.3: Spectrum of a coherently sampled, clipped ADC output data

C) Non-coherent sampling and ADC Clipping

If the input signal to ADC is simultaneously over-ranged and non-coherently sampled, the DFT of the output of such data would result in a spectrum as shown in Fig. 3.4. The spectrum not only has leakage due to non-coherent sampling but also has higher distortions due to clipped ADC output. The spectrum cannot provide accurate spectral results. As mentioned earlier, such cases could arise in BIST ADCs due to lack of precise control over amplitude and frequency of input. A test method that can accurately estimate all the spectral characteristics of ADC when the input is both over-ranged and non-coherently sampled is required.

From Fig. 3.4, it can be stated that, when DFT is performed on a non-coherently sampled, slightly clipped ADC output, the leakage and distortion in the spectrum is mainly due to the fundamental component in ADC output. The effect of non-coherent sampling can be eliminated by first accurately estimating the non-coherently sampled, over-ranged fundamental component in ADC output. The estimated fundamental is then

clipped and subtracted from the ADC output to obtain the residue. This residue contains the information of harmonics and noise of ADC (at points when the ADC output is not clipped). Fig. 3.5 shows the spectrum of residue and it can be seen that leakage is eliminated.

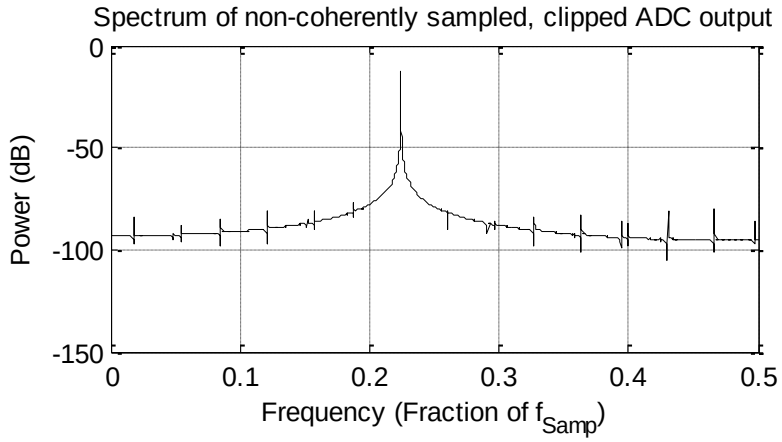

Figure 3.4: Spectrum of a non-coherently sampled and clipped ADC output.

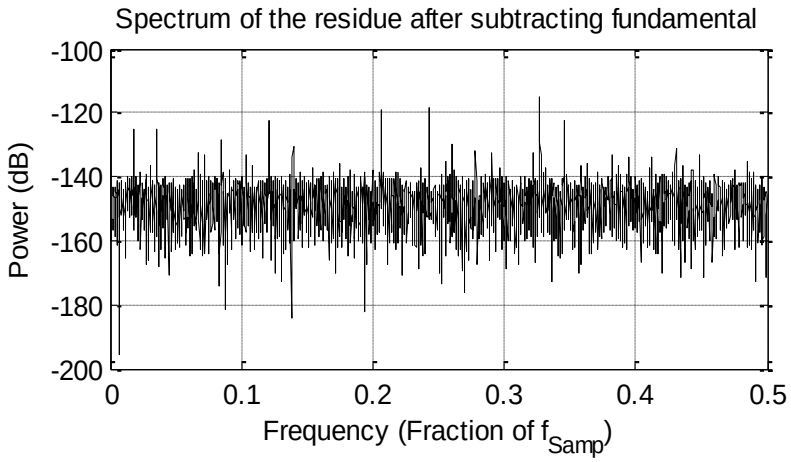

Figure 3.5: Spectrum of the residue obtained after subtracting the non-coherently sampled, over-ranged fundamental from ADC output in Fig. 3.4. Leakage due to non-coherent sampling is eliminated.

The effect of clipping can be removed by constructing a coherently sampled, unclipped fundamental signal and adding the information of harmonics and noise at each code hit by the newly constructed fundamental. This information of harmonics and noise can be obtained by interpolating the residue from ADC output codes that are not clipped.

To identify the fundamental in clipped ADC output data, methods described in [10-11] or in chapter 2 cannot be used as they do not consider the effect of clipping. The methods were used for high resolution spectral testing where the distortion power is negligible compared to that of the fundamental power. However, in presence of clipping, the distortion power is no longer negligible compared to that of the fundamental. So, a new fundamental identification method is required that is valid for clipped data. In the following section, a method to accurately estimate the spectral characteristics of an ADC when an input is non-coherently sampled and is over-ranged is proposed. A new method to identify the fundamental component in a non-coherently sampled, clipped ADC output data is described. The process of interpolating the residue is explained in detail.

III. FUNDAMENTAL ESTIMATION, REMOVAL AND RESIDUE INTERPOLATION (FERARI) METHOD

Let $x[n]$ be the n^{th} sampled point of $X(t)$. Let $y_A[n]$ be the analog interpretation of n^{th} sampled digital output of ADC whose gain and offset are corrected. From (3.1), (3.2), (3.3), (3.4) and noting that the over-range up to 2% is considered, $x[n]$ and $y_A[n]$ can be represented by equations (3.5-3.6) respectively. $y_A[n]$ is obtained after considering only first H harmonics and neglecting the higher order harmonics as their power is negligible.

$$x[n] = V_{OS} + A\cos\left(\frac{2\pi J}{M}n + \phi\right) \tag{3.5}$$

$$\begin{aligned} y_A[n] &= \begin{pmatrix} V_{OS} + A\cos\left(\frac{2\pi J}{M}n + \phi\right) \\ +\sum_{h=2}^{H} A_h \cos\left(\frac{2\pi hJ}{M}n + \phi_h\right) + w[n] \end{pmatrix} && \text{if } 0 \le x[n] \le V_{ADC} \\ &= 0 && \text{if } x[n] \le 0 \\ &= V_{ADC} && \text{if } x[n] \ge V_{ADC} \end{aligned} \tag{3.6}$$

for n = 0,1,2,….,M-1, *w[n]* is the noise in n[th] sample, ϕ is the initial phase at which the signals $\boldsymbol{x}$ and $\boldsymbol{y_A}$ are sampled. A_h and ϕ_h respectively contain the information of amplitude and phase of h[th] harmonic of ADC such that $A_h << A$ and $\phi_h \epsilon (0\ 2\pi]$. M is selected to be a power of 2 for faster processing of Fast Fourier Transform (FFT).

Before the fundamental is identified, in order to test ADC within the input range given by [F_b F_t], equation (3.6) can be changed to (3.7). This includes clipping the values of $\boldsymbol{y_A}$ that are not in the ADC input range. It should be noted that if $F_t = V_{ADC}$ and $F_b = 0$, equation (3.6) is equal to equation (3.7).

$$\begin{aligned} y[n] &= y_A[n] && \text{if } F_b \le y_A[n] \le F_t \\ &= F_b && \text{if } y_A[n] < F_b \\ &= F_t && \text{if } y_A[n] > F_t \end{aligned} \tag{3.7}$$

The sample waveforms of $\boldsymbol{x}$ and $\boldsymbol{y}$ are shown in Fig. 3.6. As input $\boldsymbol{x}$, exceeds the input range of ADC, $\boldsymbol{y}$ is clipped. With this clipped data, the fundamental component is estimated as described in the following section.

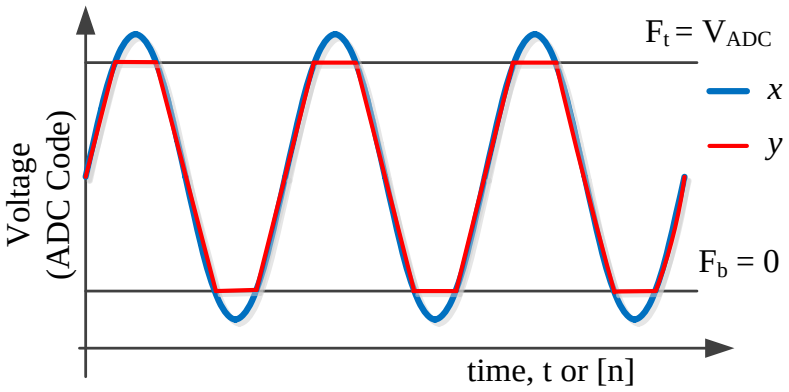

Figure 3.6: Plot showing a sample waveform of input to ADC, **x** (Eq. 3.5) and modified output of ADC, **y** (Eq. 3.7).

A) Fundamental Identification

From (3.6-3.7), in order to identify the fundamental, it is required to estimate V_{OS}, A, J_{int}, δ and ϕ. All the five parameters can be estimated using both time domain and frequency domain data. It should be noted that there is no information of fundamental or harmonics in the points that are clipped.

1. Estimate A and V_{OS}

From equations (3.6-3.7), it can be seen that $\boldsymbol{y}$ contains J cycles of the input signal. All the points in $\boldsymbol{y}$ and $\boldsymbol{x}$ are folded in to a single cycle as shown in Fig. 3.7 to obtain $\boldsymbol{y_1}$ and $\boldsymbol{x_1}$ as given by (3.8-3.9) respectively. The effect of harmonics is neglected since $A_h << A$. ϕ is the initial phase of fundamental that is sampled in $\boldsymbol{x_1}$.

$$x_1[n] = V_{OS} + A\cos\left(\frac{2\pi}{M}n + \phi\right) \tag{3.8}$$

$$y_1[n] = V_{OS} + A\cos\left(\frac{2\pi}{M}n + \phi\right) \quad \text{if } F_b \le x_1[n] \le F_t$$
$$= F_b \quad \text{if } x_1[n] < F_b \qquad (3.9)$$
$$= F_t \quad \text{if } x_1[n] > F_t$$

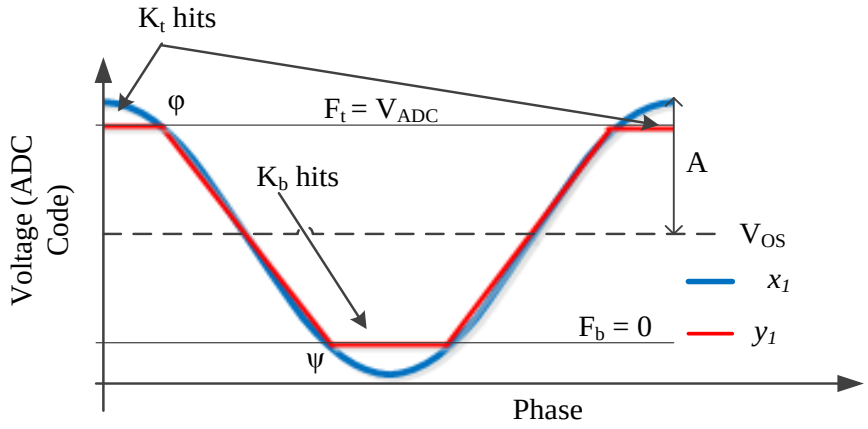

Figure 3.7: Plot showing signals $\mathbf{x_1}$ and $\mathbf{y_1}$ after folding **x** and **y** in to one cycle. K_t and K_b are total number of points in $\mathbf{y_1}$ (or **y**) equal to F_t and F_b respectively.

Let K_t and K_b be the total number of points in $\boldsymbol{y_1}$ that are equal to F_t and F_b respectively. Let φ and ψ be the phases in $\boldsymbol{y_1}$ when the clipping stops at F_t and clipping starts at F_b respectively as shown in Fig. 3.7. Using K_t and K_b, the values of φ and ψ are obtained from equation (3.10).

$$\varphi = \frac{K_t - 1}{M}\pi; \qquad \psi = \frac{K_b - 1}{M}\pi; \qquad (3.10)$$

Substituting F_t and F_b for $\boldsymbol{y_1}$ in (3.9) at phases φ and ψ respectively, the values of A and V_{os} can be estimated (3.11-3.12).

$$A = \frac{F_t - F_b}{\cos\left(\frac{K_t - 1}{M}\pi\right) + \cos\left(\frac{K_b - 1}{M}\pi\right)} \tag{3.11}$$

$$V_{OS} = \frac{F_t + F_b + A\left\{\cos\left(\frac{K_b - 1}{M}\pi\right) - \cos\left(\frac{K_t - 1}{M}\pi\right)\right\}}{2} \tag{3.12}$$

It should be noted that it is not required to perform this folding operation in the algorithm. It was used only to elucidate the procedure to estimate A and V_{OS}. From (3.11-3.12), to estimate A and V_{OS}, the values of F_t, F_b, K_t and K_b are required. F_t and F_b are known from the input range of ADC while K_t and K_b can be obtained by processing $\boldsymbol{y}$ directly.

2. Estimate J_{int}, δ and ϕ

The remaining three parameters are estimated using both time and frequency domain data of $\boldsymbol{y}$. DFT is applied on $\boldsymbol{y}$ to obtain Y_k {k^{th} DFT coefficient} given by (3.13).

$$Y_k = \sum_{n=0}^{M-1} y[n] e^{-j\frac{2\pi k}{M}n}, \quad for\ k = 0,1,2,\ldots,M-1 \tag{3.13}$$

J_{int} is estimated as the bin index that has the maximum power in half spectrum excluding DC component and is given by equation (3.14).

$$J_{\text{int}} = \underset{1 \le k \le (M/2)}{\arg\max} |Y_k| \tag{3.14}$$

From [15], to obtain the initial estimates of δ and ϕ, for M>1024, Y_k is given as (3.15) (similar to the procedure performed in chapter 2).

$$Y_k \approx \frac{A}{2M} e^{j\phi} \frac{1-e^{j2\pi(J-k)}}{1-e^{j\frac{2\pi(J-k)}{M}}} \tag{3.15}$$

Using Y_{Jint}, Y_{Jint+1} and Y_{Jint-1}, from (3.15), the initial values of δ and ϕ can be obtained using (3.16-3.17) respectively.

$$\delta_0 = \frac{M}{2\pi} imag\left(\ln\left(\frac{\frac{Y_{J_{\text{int}}}}{Y_{J_{\text{int}}+1}} - \frac{Y_{J_{\text{int}}}}{Y_{J_{\text{int}}-1}}}{\frac{Y_{J_{\text{int}}}}{Y_{J_{\text{int}}+1}} - \frac{Y_{J_{\text{int}}}}{Y_{J_{\text{int}}-1}} + e^{j\frac{2\pi}{M}} - e^{-j\frac{2\pi}{M}}} \right) \right) \tag{3.16}$$

$$\phi_0 = -imag\left(\ln\left(\frac{2MY_{J_{\text{int}}}}{A} \frac{1-e^{j\frac{2\pi\delta_0}{M}}}{1-e^{j2\pi\delta_0}} \right) \right) \tag{3.17}$$

Since, Y_k corresponds to a non-coherently sampled data, the values of δ and ϕ obtained are not accurate. Let $\Delta\delta$ ($=\delta-\delta_0$) and $\Delta\phi$ ($=\phi-\phi_0$) correspond to errors in estimating δ and ϕ using (3.16-3.17) respectively. It is required to estimate these errors in order to improve the accuracy of estimated δ and ϕ.

Substituting the estimated values in $\boldsymbol{y}$ (eq. 3.7) gives equation (3.18) and rearranging the terms, we get (3.19). The effect of harmonics is neglected and "n" in (3.18-3.19) correspond to the samples that are not clipped. The points in $\boldsymbol{y}$ that are close to V_{os} (mid-range codes) are considered in (3.19) as shown in Fig. 3.8. These points are considered because, they are linear in the range and give good estimates of $\Delta\delta$ and $\Delta\phi$ when Least squares is applied on (3.19). After estimating $\Delta\delta$ and $\Delta\phi$, using (3.11-3.12), (3.14), (3.16-3.17) the initial estimated fundamental, $\boldsymbol{z_i}$, is given by (3.20).

$$y[n] = V_{OS} + A\cos\left(\frac{2\pi\left(J_{\text{int}} + \delta_0 + \Delta\delta\right)}{M}n + \phi_0 + \Delta\phi\right) \tag{3.18}$$

$$\frac{2\pi n}{M}\Delta\delta + \Delta\phi = \cos^{-1}\left(\frac{y[n] - V_{OS}}{A}\right) - \phi_0 - \frac{2\pi\left(J_{\text{int}} + \delta_0\right)n}{M} \tag{3.19}$$

$$z_i[n] = V_{OS} + A\cos\left(\frac{2\pi\left(J_{\text{int}} + \delta_0 + \Delta\delta\right)}{M}n + \left(\phi_0 + \Delta\phi\right)\right) \tag{3.20}$$

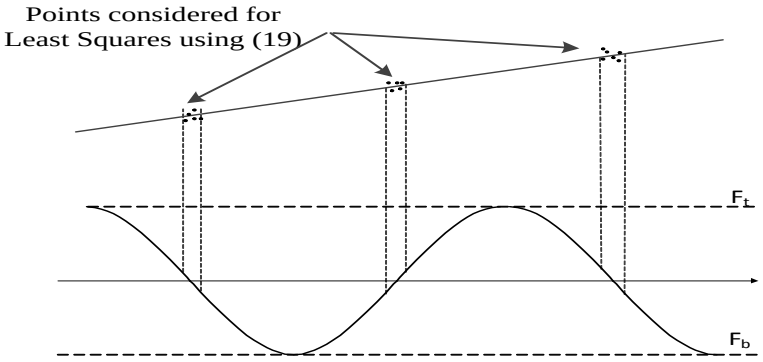

Figure 3.8: Plot showing signal **y** and the points considered for Least squares using equation (3.19). Only output codes around mid-range are considered.

To further improve the accuracy in estimating *A*, let ΔA be the error in estimating *A* (eq. 3.11). ΔA can be estimated by first clipping $\boldsymbol{z_i}$ to obtain $\boldsymbol{z_{ic}}$ and subtracting $\boldsymbol{z_{ic}}$ from ADC output, ***y,*** to obtain the error signal, ***ez*** as shown in (3.21-3.22). Later, DFT is applied on ***ez*** and the fundamental amplitude in ***ez***, ΔA, is estimated using (3.23). $\tilde{Y}_k$ in (3.23) is the k^{th} DFT coefficient of ***ez***. Now the actual fundamental component in ***y*** can be estimated as ***z*** using (3.24) and is shown in Fig. 3.9a (green dotted plot).

$$\begin{aligned} z_{ic}[n] &= z_i[n] \quad \text{if } F_b \le z_i[n] \le F_t \\ &= F_b \quad \text{if } z_i[n] < F_b \\ &= F_t \quad \text{if } z_i[n] > F_t \end{aligned} \tag{3.21}$$

$$ez[n] = y[n] - z_{ic}[n] \tag{3.22}$$

$$\Delta A = 2M \left| \tilde{Y}_{J_{\text{int}}} \right| \left| \frac{1 - e^{j\frac{2\pi\delta_0}{M}}}{1 - e^{j2\pi\delta_0}} \right| \tag{3.23}$$

$$z[n] = z_i[n] + \Delta A \cos\left(\frac{2\pi\left(J_{\text{int}} + \delta_0 + \Delta\delta\right)}{M} n + \left(\phi_0 + \Delta\phi\right) \right) \tag{3.24}$$

Since, non-coherently sampled fundamental is the major source of error, subtracting the estimated fundamental, ***z***, from ADC output, ***y***, eliminates the effect of non-coherent sampling.

B) Obtain Error (Harmonics + Noise of ADC) Information

The residue, ***e***, obtained after subtracting the estimated fundamental, ***z,*** from modified ADC output, ***y,*** is shown in Fig. 3.9b. It can be seen that the blocked regions contain no information about the ADC non-linearity as the input signal is not in the ADC input range. So, the information of harmonics and noise of ADC is present only in the points that are not clipped in ***y***. In order to include the dynamic effects of ADC, the error voltage, ***e*** in Fig. 3.9b, is separated into two categories, FP and RP which correspond to the error voltage when the input signal is falling and rising respectively as shown in Fig. 3.9b. The error voltage in FP and RP categories is separated to be ***ef*** and ***er*** respectively. From Fig. 3.9a and 3.9b, for each sample in RP, the value of *er[n]* is plotted with respect

to corresponding *y[n]* as shown in Fig. 3.10b. Similarly, *ef[n]* is plotted with respect to *y[n]* as shown in Fig. 3.10a. With this, error in both phases (Rising and Falling) with respect to the code hit by ADC is obtained. This error contains the information of harmonics and noise of ADC.

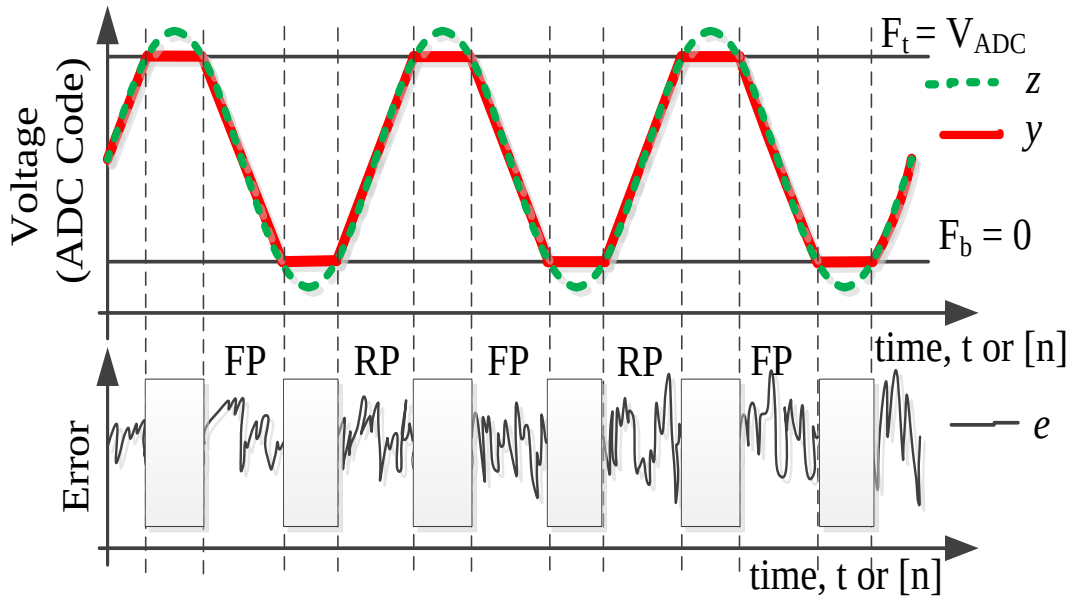

Figure 3.9: a): TOP :- Figure showing ADC output, **y** and estimated fundamental, **z**.
b) BOTTOM :- Figure showing the error (Harmonics + Noise) information, **e**, of ADC.
(RP: Rising Phase, FP: Falling Phase, Blocked: Neglect).

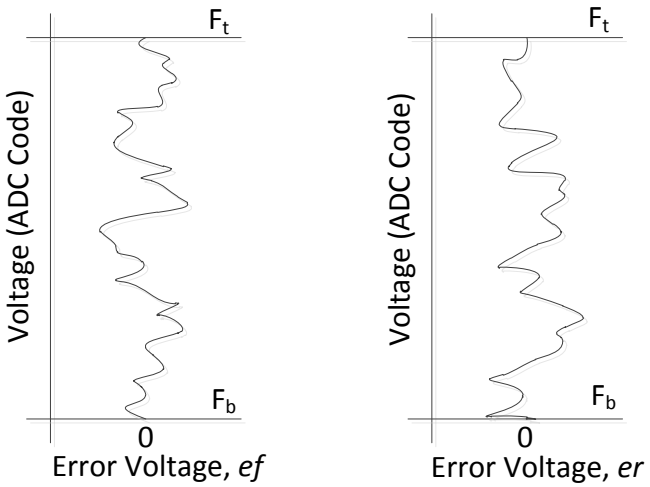

Figure 3.10: a) LEFT:- Plot of error in FP, **ef** versus ADC output code, **y**. b) RIGHT:- Plot of error in RP, **er** versus ADC output code, **y**.

C) Coherent Time Domain data Reconstruction

With the information of $J_{int,}$ ϕ and ADC range (F_t and F_b), the input signal that is coherently sampled and covers the input range of ADC (without clipping) is obtained and is given by $\boldsymbol{v}$ in (3.25). It is required to add the information of harmonics of ADC on to each sample of the coherent fundamental $\boldsymbol{v}$ to accurately estimate the spectral characteristics of ADC.

It should be noted that the codes hit in ADC output, $\boldsymbol{y}$, are not the same codes that are hit using $\boldsymbol{v}$ (Coherent, unclipped). To obtain the errors corresponding to each code in $\boldsymbol{v}$, first, all points in $\boldsymbol{v}$ are folded into one cycle to get $\boldsymbol{v_1}$ given by (3.26) as shown in Fig. 3.11 (blue). Also, shown in Fig. 3.11 is the folded ADC output $\boldsymbol{y_1}$ (red). The information of error for each sampled point in the falling phase of $\boldsymbol{v_1}$ is obtained by using $\boldsymbol{ef}$ as shown in Fig. 3.12 (blue straight lines). For each sampled point in falling phase of $\boldsymbol{v_1}$ ($v_1[c]$), two codes in $\boldsymbol{y_1}$ ($y_1[a]$ and $y_1[b]$) that are in the falling phase and close to $v_1[c]$ are used

and interpolation of the two errors at those codes (*ef[a]* and *ef[b]*) is performed to estimate the error at code $v_1[c]$ (given as *ev[c]*). The interpolation equation is as shown in equation (3.27). Similarly, the error information for the rising phase of $\boldsymbol{v_1}$ can be obtained by interpolating ***er*** (Red straight lines in Fig. 3.12).

$$v[n] = \frac{F_t + F_b}{2} + \frac{F_t - F_b}{2}\cos\left(\frac{2\pi J_{\text{int}}}{M}n + \phi\right) \tag{3.25}$$

$$v_1[n] = \frac{F_t + F_b}{2} + \frac{F_t - F_b}{2}\cos\left(\frac{2\pi}{M}n + \phi\right) \tag{3.26}$$

$$ev[c] = ef[a] + \frac{(ef[b] - ef[a])}{(y_1[b] - y_1[a])}(v_1[c] - y_1[a]) \tag{3.27}$$

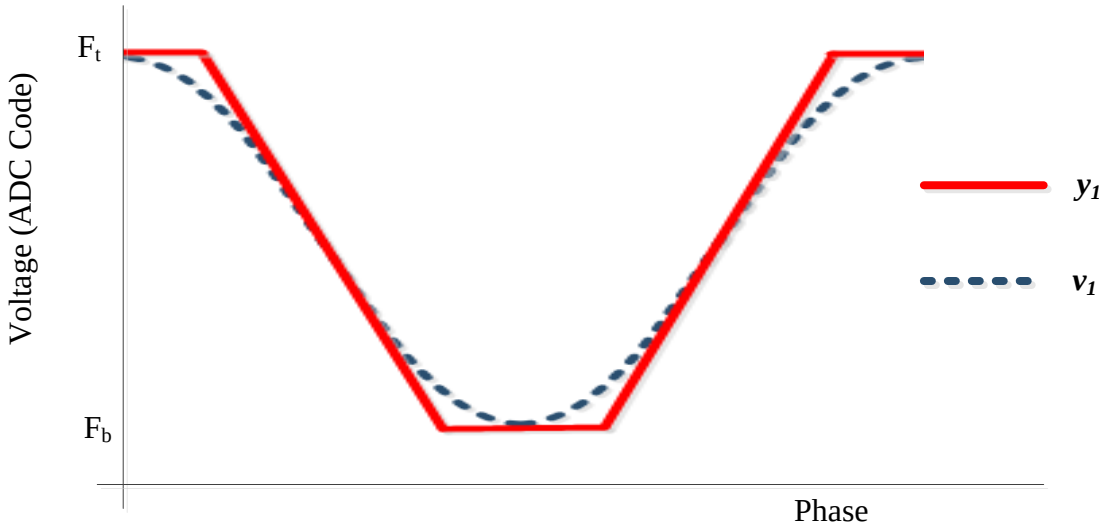

Figure 3.11: Figure showing folded ADC output, $\mathbf{y_1}$ and folded coherent signal, $\mathbf{v_1}$.

The information of error obtained for each code hit by v_1 (in both rise and fall phases) is then added to v_1 to get f_1. f_1 is then unfolded into J_{int} cycles to obtain f. It should be noted that f contains not only the information of coherent fundamental but also the accurate information of harmonics and noise of ADC. Taking FFT of f would result in a spectrum that looks identical to the spectrum obtained using ideal test setup. Hence, accurate spectral characteristics of ADC can be obtained even with non-coherently sampled and clipped data using proposed method.

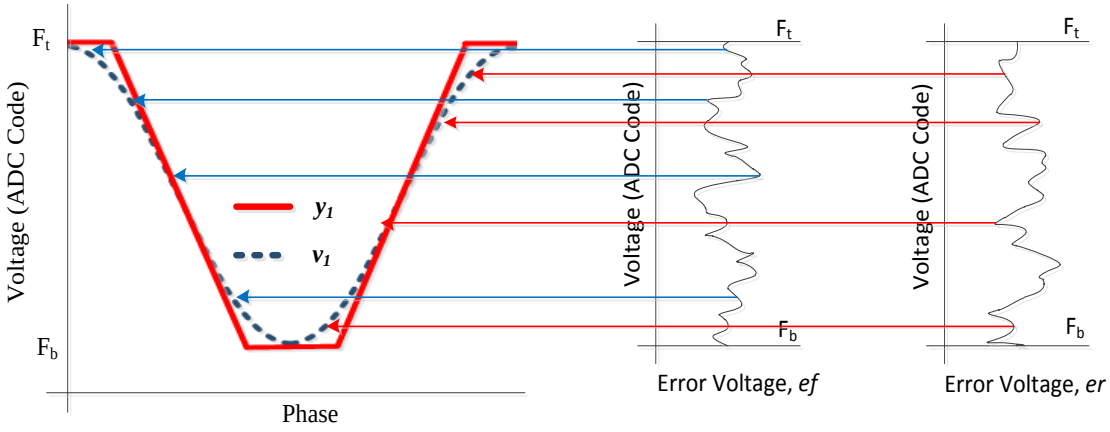

Figure 3.12: Figure illustrating the interpolation of error onto $\mathbf{v_1}$. Error in **ef** is interpolated onto points in $\mathbf{v_1}$ in falling phase (Here left half of $\mathbf{v_1}$) while error in **er** is interpolated onto points in $\mathbf{v_1}$ in rising phase (Here right half of $\mathbf{v_1}$)

It can be argued that the dV/dt effects are not the same for both the signals y and v (from Fig. 3.11). However, since in this chapter, only 2% over-range is considered, it can be mentioned that the dV/dt effect on harmonics' estimation is negligible.

D) Need for Interpolation

It should be noted that the step to perform interpolation for each point on the coherently sampled data (***v***) is important to test high resolution ADCs. If interpolation is not performed, the residue obtained (after clipping and subtracting the estimated fundamental from the clipped ADC output) is directly added to the coherently sampled fundamental, ***v***, to obtain final data. DFT is performed on this data to perform spectral test. Let this process be called "Method B". Method B can be used only when the power associated with the clipped points is less than the noise power of the ADC. Hence Method B can be used to test only low resolution ADCs. However, as the resolution of ADC increases, the noise power of ADC decreases and Method B cannot be used. For instance, consider testing a 12-bit ADC and 16-bit ADC with non-coherently sampled, 1.7% over-ranged input signal. The spectral results obtained using three methods are given in Table 3.1 and Table 3.2. The first method is the standard method with unclipped and coherently sampled ADC output. The second method is using Method B and the third method is using the proposed method on the same ADC with non-coherently sampled, over-ranged input. From Tables 3.1 and 3.2, it can be seen that Method B provides accurate results only for the 12-bit ADC. However, the proposed method can be used to test both low and high resolution ADCs accurately. Hence, it is important to perform residue interpolation to obtain accurate spectral results when an input to ADC is over-ranged and is non-coherently sampled.

TABLE 3.1: Spectral results of a 12-bit ADC

Method	THD (dB)	SFDR (dB)
Coherent Unclipped (Reference)	-70.3	73.9
Method B (No interpolation)	-70.5	74.7
Proposed Method(With Interpolation)	-70.8	74.3

TABLE 3.2: Spectral results of a 16-bit ADC

Method	THD (dB)	SFDR (dB)
Coherent Unclipped (Reference)	-93.1	97.7
Method B (No interpolation)	-79.7	84.2
Proposed Method (With Interpolation)	-93.3	97.7

The flow chart to perform accurate ADC spectral testing with non-coherent sampling and over-ranged input using the proposed FERARI method is shown in Fig. 3.13. The steps in solid rectangle can be used when the output is non-coherently sampled while the steps in dotted rectangle can be used when the output is clipped.

E) Comparison with Four Parameter Sine Fit Method

The fundamental identification method in Section A can be replaced with the four parameter sine fit method as described in [8] with slight modification. Both the methods provide accurate estimates of the fundamental. However, the proposed method is more computationally efficient than the four parameter sine fit method. Using four parameter sine fit method, all unclipped points in data are considered to perform non-linear least squares. This includes large data set and several iterations to obtain

convergence which consumes large computation time. However, in the proposed method, the time consuming blocks are FFT and linear least squares method. As M is usually selected to be a power of 2, FFT consumes very small amount of time. Since a very small number of points around the mid-range codes are considered for linear least squares (as shown in Fig. 3.8), this operation also does not consume more time. The other factor which makes the proposed method more time efficient compared to the four parameter sine fit method is that, there is no necessity to perform iterations.

IV. SIMULATION RESULTS

The accurate functionality and robustness of the proposed method is shown using simulation results in this section.

A) Functionality

A 16-bit ADC with INL of 1.5LSB was generated using MATLAB. A total of 8192 points were sampled. The ADC was first tested with a sine wave that is coherently sampled and not clipped. The signal is generated such that it covers the ADC input range without getting clipped. The values of THD and SFDR obtained are considered as the reference values. The same ADC is later fed with an over-ranged, non-coherently sampled input signal. The output is processed using the proposed method and the values of THD and SFDR are compared.

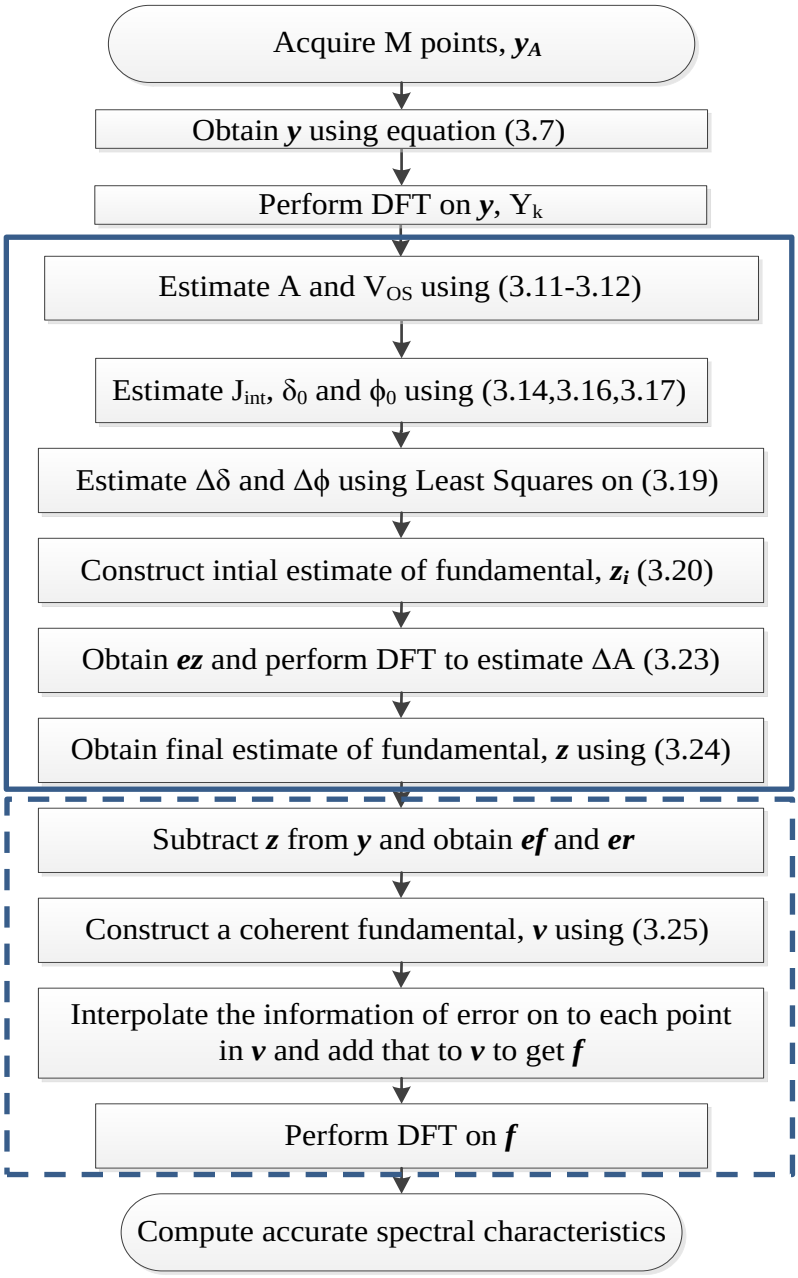

Figure 3.13: Flow chart to perform accurate ADC spectral test using proposed method on Non-coherently sampled, clipped ADC output. Solid rectangle steps used when signal is non-coherently sampled. Dotted rectangle steps used when output is clipped.

Fig. 3.14 shows the spectrum of ADC output when it is coherently sampled. The value of J = 3241. It can be seen that there is no leakage in the spectrum and the values of THD and SFDR obtained are listed in Table 3.3. Fig. 3.15 shows the spectrum of the same ADC output when a non-coherently sampled, over-ranged input signal is fed to the ADC. The value of J is 3241.199 and over-range is 0.78%. It can be seen that there is both leakage and severe distortion in the spectrum. Later the same ADC output is processed using the proposed method and the spectrum obtained is as shown in Fig. 3.16. The spectrum is clean and it exactly matches with the spectrum obtained using coherent sampling. The values of THD and SFDR obtained using proposed method are listed in Table 3.3. From Table 3.3 and Fig. 3.16, it can be said that the proposed method accurately estimates the THD and SFDR of a non-coherently sampled, clipped ADC output.

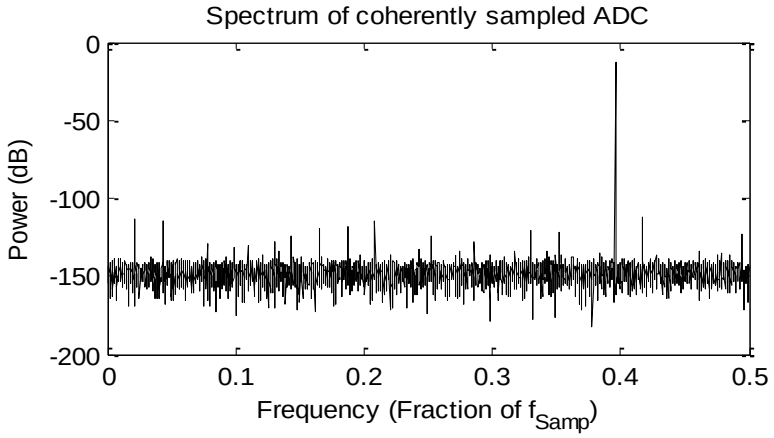

Figure 3.14: Spectrum of a coherently sampled, unclipped ADC output (J = 3241)

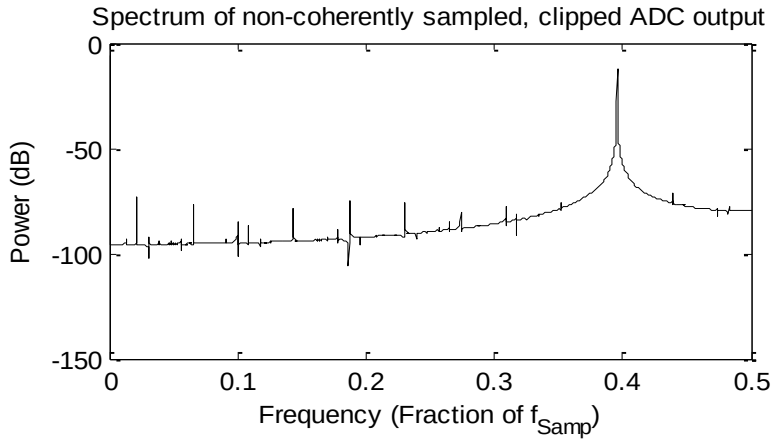

Figure 3.15: Spectrum of DFT of a non-coherently sampled, clipped ADC output (J = 3241.199 → δ = 0.199, %over-range = 0.78)

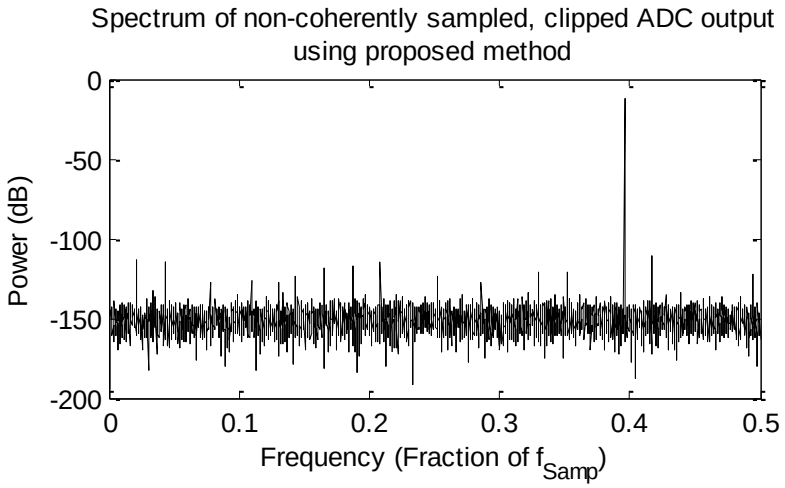

Figure 3.16: Spectrum of a non-coherently sampled, clipped ADC output after using the proposed FERARI method (J=3241.199→ δ = 0.199, % Over-range = 0.78)

TABLE 3.3: Spectral results of 16-bit ADC (Fig. 3.14 & Fig. 3.16)

Method	**THD (dB)**	**SFDR (dB)**
Coherent + Unclipped + DFT	-93.7	99.2
Non-coherent+Clipped + FERARI	-94.1	99.2

B) Robustness

The robustness of proposed method is shown with respect to non-coherent sampling and amplitude clipping up to 2%. A 16-bit ADC was generated using MATLAB with an INL of 1.8 LSB. A total of 500 runs with randomly selected values of δ and over-range were run. The values of δ vary from -0.5 to 0.5 (total range) and over-range percentage was in the range 0 to 2. The data record length for each run was 8192. Fig. 3.17 and Fig. 3.18 show the errors in estimating the values of THD and SFDR with δ respectively. Fig. 3.19 and Fig. 3.20 show the errors in THD and SFDR with percent input over-range respectively. The maximum error obtained in estimating THD and SFDR is about 1dB. This shows that the method is robust to both non-coherent sampling and amplitude over-range up to 2%.

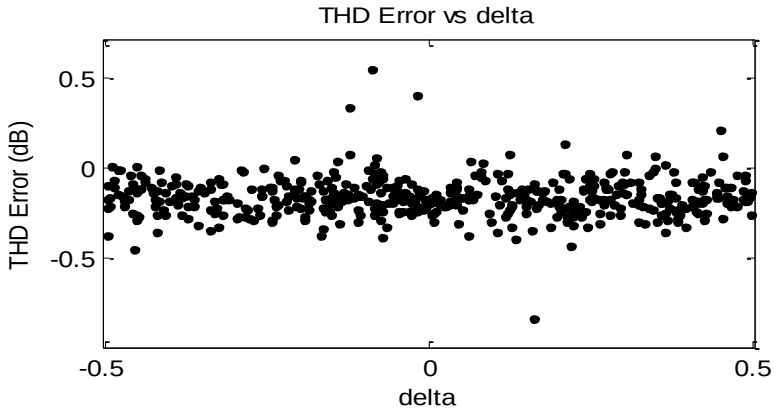

Figure 3.17: Error in estimating THD values (in dB) using FERARI method over whole range of δ.

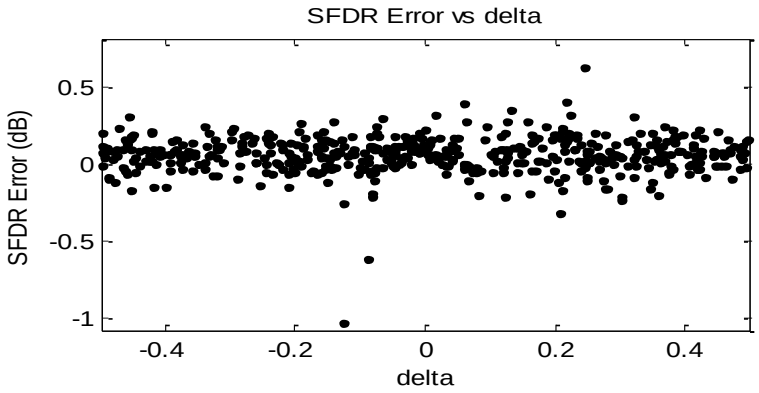

Figure 3.18: Error in estimating SFDR values (in dB) using proposed FERARI method over whole range of δ.

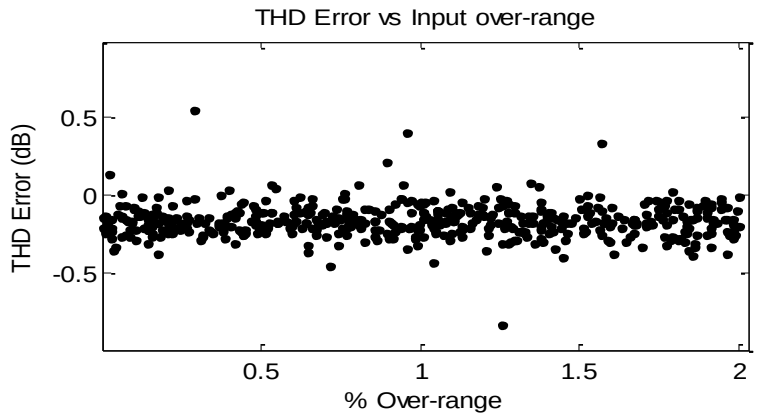

Figure 3.19: Error in estimating THD values (in dB) using proposed FERARI method for different input over-range amplitudes.

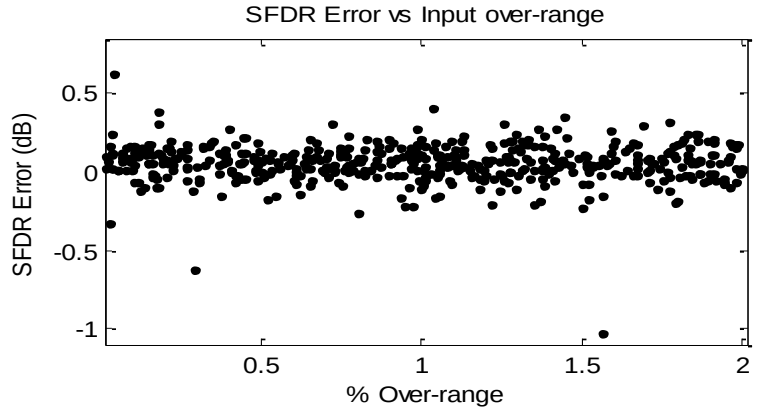

Figure 3.20: Error in estimating SFDR values (in dB) using FERARI method for different input over-range amplitudes.

V. MEASUREMENT RESULTS

In this section, the proposed method is verified using measurement results from industry labs using a commercially available high resolution ADC.

The ADC that is used is ADS8318 which is a 16-bit Successive Approximation Register (SAR) ADC clocked at 500 kSPS. The input range of ADC is 0 to 5V. Fig. 3.21 shows the test setup. The input signal is followed by two band pass filters each with center frequency at 10 kHz. The output of the second band pass filter is fed to the input of ADC. A total of 8192 samples are collected.

The input frequency to achieve coherent sampling is given by 10.070800781 kHz which gives a value of J = 165. The blue spectrum in Fig. 3.22 shows the spectrum obtained using coherently sampled and unclipped data. It can be seen that there is no leakage in the spectrum.

Later, the frequency of input signal is changed to 10.049476891 kHz and the input amplitude is slightly increased to be about 1.5% more than the ADC input range. As a result, the input signal is both non-coherently sampled (J=164.65, $\delta \approx -0.35$) and over-ranged (1.5%). The green plot in Fig. 3.22 shows the spectrum obtained without any correction. As expected, there is huge spectral leakage and higher distortion in the spectrum. The same time domain data is then processed using the proposed method. The red plot in Fig. 3.22 shows the spectrum obtained using the proposed FERARI method. It can be seen that the red spectrum (Non-coherent + Clipped + Proposed method) matches exactly with that of the blue spectrum (Coherent + Unclipped). The values of THD, SFDR and SNR obtained using standard coherent sampling method on unclipped

data and proposed method on non-coherently sampled, clipped data are listed in Table 3.4. From Table 3.4 and Fig. 3.22, the accurate functionality of the proposed method with non-coherently sampled and over-ranged input is verified.

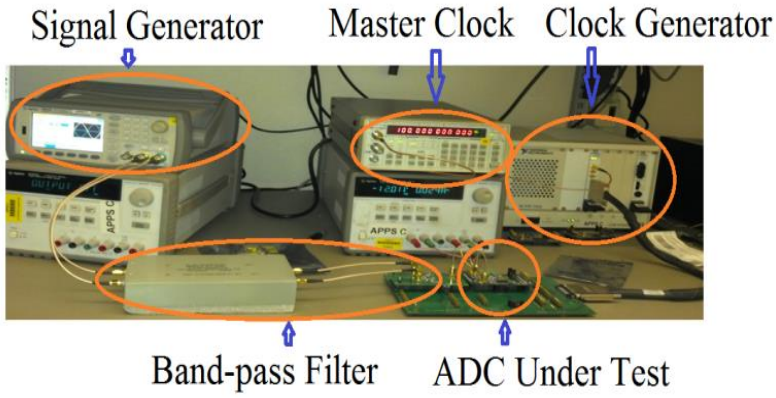

Figure 3.21: Test setup for Measurement data of ADS8318.

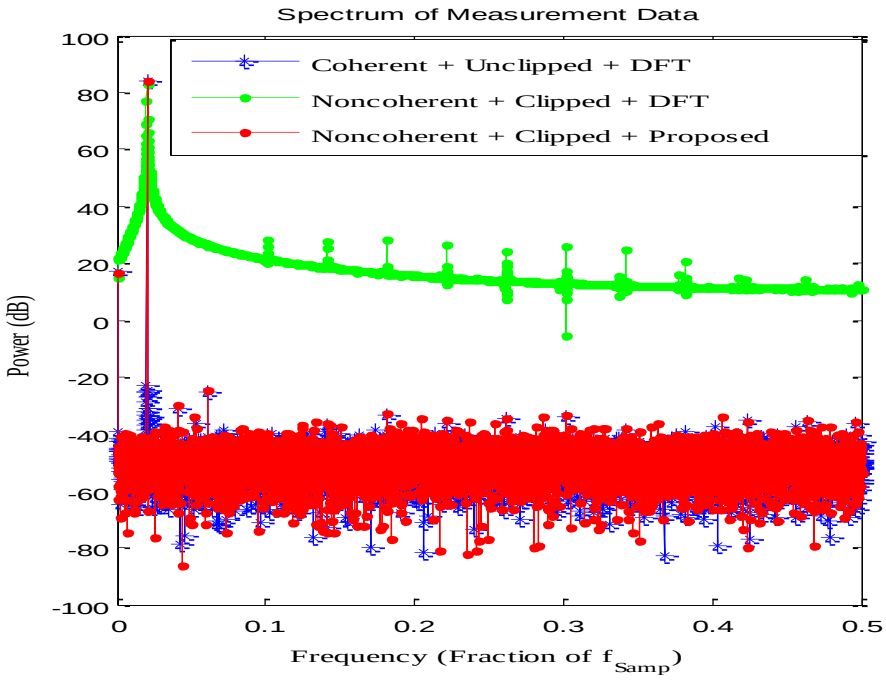

Figure 3.22: Spectrums showing the accurate functionality of the proposed method. BLUE: Spectrum with Coherently sampled, unclipped data, GREEN: Spectrum with clipped and non-coherently sampled data, RED: Spectrum with Non-coherently sampled, Clipped data using the proposed FERARI method. (δ=-0.35, % over-range = 1.5)

TABLE 3.4: Spectral results of ADS8318 from Fig. 3.22

Method	THD(dB)	SFDR(dB)	SNR(dB)
Non-coherent + Clipped + FERARI (Red plot in Fig. 3.22)	-107.6	109.2	95.7
Coherent + Unclipped + DFT (**Standard**, Blue plot in Fig. 3.22)	-107.5	108.5	95.8

The robustness of the proposed method is also shown using measurement data. The frequency of input signal is varied from 10.040283203 kHz to 10.101318359 kHz so that the value of J varies from 164.5 to 165.5 respectively. This covers the whole range of δ from -0.5 to 0.5. For each frequency, the input was over-ranged from 0 to 2%. As a result, the input signal to each test run is both non-coherently sampled and over-ranged. The values of THD, SFDR and SNR with different over-range levels and different values of δ are plotted in Fig. 3.23, Fig. 3.24 and Fig. 3.25 respectively. The accurate values of THD, SFDR and SNR of the ADC to be compared are given in Table 3.4 (using coherent sampling). The variation of THD and SFDR is expected as only 8192 points are sampled to test a 16-bit ADC. It can be seen that the proposed method accurately estimated the spectral parameters and is robust to any non-coherency and over-range up to 2%. As a result, the proposed method can be used for BIST applications without precise control of frequency and amplitude of test input, thus, reducing test cost.

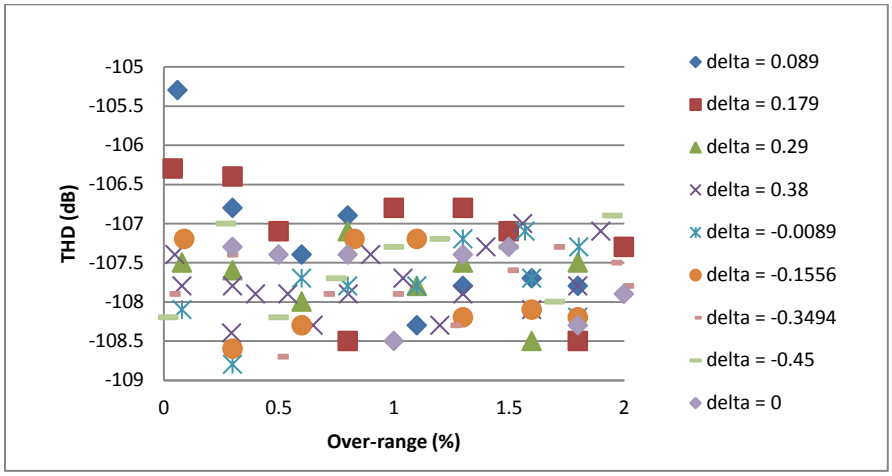

Figure 3.23: Plot showing the robustness of proposed method. THD values measured using the proposed method for various input over-range percentages and different values of δ. (THD for coherent sampling = -107.5 dB)

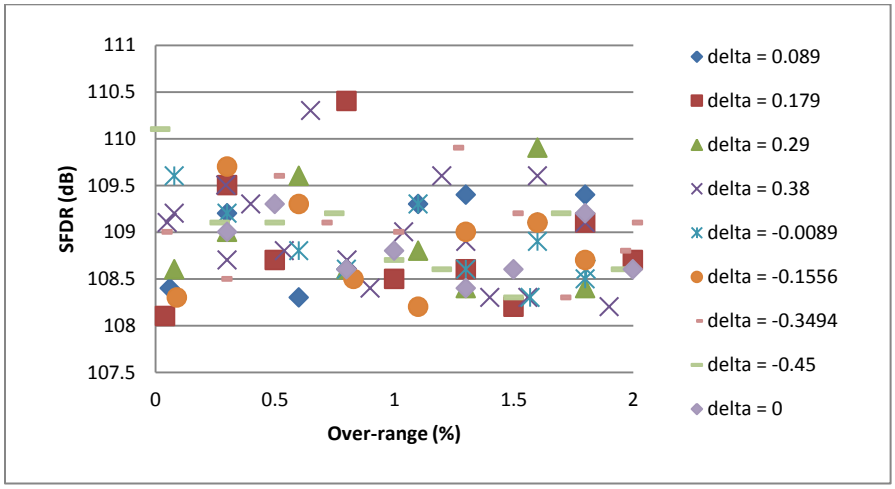

Figure 3.24: Plot showing the robustness of proposed method. SFDR values measured using the proposed method for various input over-range percentages and different values of δ. (SFDR for coherent sampling = 108.5 dB)

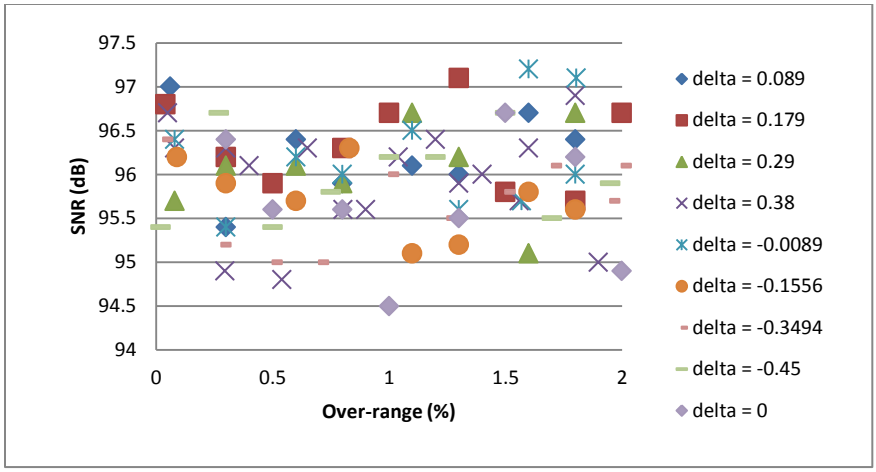

Figure 3.25: Plot showing the robustness of proposed method. SNR values measured using the proposed method for various input over-range percentages and different values of δ. (SNR for coherent sampling = 95.8 dB)

VI. CONCLUSION

A new test method that accurately estimates the spectral characteristics of an ADC with non-coherently sampled and over-ranged input was proposed. This relaxes the requirement to have precise control over frequency and amplitude of input signal for spectral testing. A new computationally efficient method to identify the over-ranged, non-coherently sampled fundamental using time domain and frequency domain data was described. The residue obtained after subtracting the estimated non-coherent fundamental is interpolated onto a coherently sampled signal to obtain accurate spectral results of ADC. The accurate functionality and robustness of the proposed method for any non-coherency and over-range up to 2% was presented using simulation results on 16-bit ADCs. The proposed method was also verified for functionality and robustness using a commercially available high resolution 16-bit SAR ADC. The method can be

readily used in applications, where in, it is challenging to obtain precise control over frequency and amplitude of test signal, such as, BIST ADCs.

VII. AKNOWLEDGMENTS

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CHAPTER 4

A LOW COST METHOD TO TEST HIGH RESOLUTION ANALOG-TO-DIGIAL CONVERTERS USING NON-LINEAR INPUT AND NON-COHERENT SAMPLING

Spectral testing is one of the most important tests performed to characterize Analog to Digital Converters (ADC). The test cost of ADC increases with increase in the resolution of ADC as, it is required to acquire a signal source that is about three to four bits more pure than the ADC. Also achieving coherent sampling is one of the major bottlenecks to perform spectral testing. In this chapter, a low-cost method is proposed that accurately estimates the spectral characteristics of a high resolution ADC using a low-cost impure (non-linear) input signal that is non-coherently sampled. A technique to characterize the nonlinear input signal when it is non-coherently sampled is explained in detail. Simulation results show that the proposed method can accurately test a 15-bit ADC using an input signal with Spurious Free Dynamic Range equal to 59dB (about 10-bit pure signal). The robustness of the proposed method with respect to any level of non-coherency is also shown.

I. INTRODUCTION

When testing an Analog to Digital Converter (ADC) for spectral parameters, the non-linearity of the ADC is tested using parameters defined in Chapter 1 such as Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR), Signal to Noise Ratio (SNR), etc. (equation 1.8). To accurately obtain the above parameters, it is ideally

required to use a pure signal source which has only one frequency called the fundamental frequency. However, in real world it is impossible to find such pure (or linear) signal sources. The signal source would be non-linear and would contain other frequency components called harmonics, which are integer multiples of the fundamental frequency. Since the signal source cannot be obtained without harmonics, it is recommended to use signal sources that have very less power in the harmonics in order to test ADCs. Typically, to test an N-bit ADC, it is recommended to use a signal source with resolution of at least N+3 bits [1]. This implies that the harmonic with maximum power in the input signal is about 10 times smaller than that of the ADC under test. With such an input, the spectral characteristics of ADC can be accurately estimated, as the harmonics in the input signal are considered negligible compared to those of the ADC.

With increase in the resolution of ADCs over time, it becomes a challenge to design very pure signal sources. For example, to test a 16-bit ADC, it is required to obtain an input sinusoid signal that has THD of about -120dB (or about 19 to 20 bit pure). This requirement on THD of the input signal keeps increasing as the resolution of ADC increases. Designing such signals is very expensive as it includes huge design effort.

Furthermore, in production test, the ADCs are tested using an Automated Test Equipment (ATE) that contains a signal source. The purity of the signal source on the ATE might not be sufficient to test a high resolution ADC. In such cases, it is required to buy a new ATE that contains a highly linear sinusoid signal generator. This results in additional test cost due to the following reasons. First, designing a high pure signal source itself is expensive and second, buying an ATE with such a signal source adds more to the

test cost. Hence, it is required to develop a test method that can relax the condition to use a pure sine source to test ADCs. Such methods could decrease the test cost.

Another challenging requirement to perform spectral testing is to achieve coherent sampling. As mentioned in Chapter 2, if the sampling is not coherent, the spectrum of the ADC output would contain severe leakage, which results in inaccurate spectral characteristics.

Over the years, work is being done to relax both the above conditions (pure input source and coherent sampling). One class of work relaxes the condition of coherent sampling alone to perform spectral testing. Such methods include windowing technique [1-4], four parameter sine fitting technique [1,5-7], filter bank method [8], resampling method [9], singular value decomposition method [10] and fundamental identification and replacement methods [11-13]. However, all the methods can be used only when the input signal is pure (that is about 10 times more pure than the ADC).

Another class of work corresponds to relaxing the condition to have highly pure input signals. Such methods could decrease the test cost by removing the design effort for building high resolution signals. In [14], a method that relaxes the above requirement was proposed. Two impure (non-linear) spectral related excitations were used as inputs to the high resolution ADC and the outputs of ADC for both excitations were processed to accurately estimate the spectral characteristics of ADC. Simulation results were presented where in a 16-bit ADC was accurately tested using a 55dB pure input signal. The proposed method however assumed coherent sampling. In [15], a similar technique was used to validate the method in [14] using experiments.

In both the above mentioned classes of work, only one of the two conditions was relaxed to perform spectral testing. However, in practical applications, it would be more cost effective if both the conditions (coherent sampling and pure input source) can be relaxed simultaneously. In this chapter, a test method that can simultaneously eliminate the requirement of both coherent sampling and pure input source to test high resolution ADCs is presented. The method is proposed from the application of production test where in a single low pure signal source is present and is non-coherently sampled to test high resolution ADCs. The remaining chapter is arranged as follows. Section II discusses the issues with non-coherent sampling and using impure sine sources. The new test method is proposed in Section III. Section IV provides simulation results and section V concludes the chapter.

II. ISSUES WITH NON-COHERENT SAMPLING AND NON-LINEAR (IMPURE) INPUT SOURCE

The procedure to perform conventional spectral testing of ADCs is provided in chapter 1. In this section, the issues with using a non-coherently sampled input and a non-linear input source to test a high resolution ADC are discussed.

A) Non-coherent sampling

The issue of non-coherent sampling is revised again in this section for ease in explanation. Considering only the effect of non-coherent sampling and assuming all the other four conditions mentioned in chapter 1 are satisfied, the following analysis is performed.

Let f_{Sig} be the frequency of input signal, f_{Samp} be the clock frequency, M be the total number of data points recorded to measure the spectral characteristics and J be the total number of periods of the input signal sampled in M points. The four parameters are related by equation (4.1).

$$J = M \frac{f_{Sig}}{f_{Samp}} \tag{4.1}$$

The M point data record is said to be sampled coherently if J in (4.1) is an integer and, if J is not an integer, it is said to be non-coherently sampled. Since, the effects of non-coherent sampling are investigated, in this section J is considered to be a non-integer.

Let $x(t)$ be the pure input to ADC under test and is given by equation (4.2). Here A is the amplitude of the fundamental and $w(t)$ is the noise at time t.

$$x(t) = A\cos\left(2\pi f_{Sig} t\right) + w(t) \tag{4.2}$$

Let $x[n]$ be the analog representation of nth digital output of ADC. $x[n]$ is given by (4.3) after calibrating for offset and gain error. Also, the higher order harmonics in the output of ADC are neglected in (4.3). Only the first H harmonics are considered for analysis as mentioned in chapter 1.

$$x[n] = A\cos\left(\frac{2\pi J}{M} n + \phi\right) + \sum_{h=2}^{H} A_h \cos\left(\frac{2\pi h J}{M} n + \phi_h\right) + w[n] \tag{4.3}$$

where ϕ is the initial phase at which the ADC output is sampled, A_h and ϕ_h are the amplitude and the initial phase of hth harmonic of ADC respectively. For non-coherent sampling, J in (4.3) is not an integer.

The output of ADC, *x[n]*, in (4.3) can also be represented by the following equations (4.4 – 4.5).

$$x[n] = A\cos\left(\frac{2\pi J}{M}n + \phi\right) + \sum_{h=2}^{H}\left(a_h \cos\left(\frac{2\pi hJ}{M}n + h\phi\right) + b_h \sin\left(\frac{2\pi hJ}{M}n + h\phi\right)\right) + w[n] \quad (4.4)$$

$$x[n] = \begin{pmatrix} a_1 \cos\left(\frac{2\pi J}{M}n\right) + b_1 \sin\left(\frac{2\pi J}{M}n\right) \\ +\sum_{h=2}^{H}\left(a_h \cos\left(\frac{2\pi hJ}{M}n + h\phi\right) + b_h \sin\left(\frac{2\pi hJ}{M}n + h\phi\right)\right) + w[n] \end{pmatrix} \quad (4.5)$$

where a_1 and b_1 contain the information of amplitude and phase of fundamental, a_h and b_h contain the amplitude and phase information of hth harmonic in ADC. It can be seen that all the three equations are different representations for the same ADC output. The parameters in the three equations are related by equations (4.6 – 4.9)

$$A = \sqrt{a_1^2 + b_1^2} \quad (4.6)$$

$$\phi = \tan^{-1}\left(\frac{a_1}{b_1}\right) \quad (4.7)$$

$$A_h = \sqrt{a_h^2 + b_h^2} \quad (4.8)$$

$$\phi_h = h\phi + \tan^{-1}\left(\frac{a_h}{b_h}\right) \quad (4.9)$$

For convenience, in this chapter the output equation represented by (4.4) is considered for analysis. To obtain the spectrum of this ADC output, DFT is performed on equation (4.4) to obtain X_k given by (4.10). X_k is the DFT coefficient of kth frequency bin.

$$X_k = \frac{1}{M}\sum_{n=0}^{M-1} x[n] e^{-j\frac{2\pi k}{M}n}, \; for \; k = 0,1,2,...,M-1 \tag{4.10}$$

Since non-coherent sampling is considered, J in (4.4) can be given as the sum of J_{int} and δ, where J_{int} is the integer part of J and δ is the non-integer part of J. Using this J and substituting equation (4.4) in (4.10) and simplifying, the k[th] DFT coefficient can be given as shown in equation (4.11).

$$X_k = \left(\begin{array}{l} \dfrac{A}{2M}\left\{ \dfrac{\sin\left(\pi\left(J_{\text{int}}+\delta-k\right)\right)}{\sin\left(\dfrac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)} e^{j\left(a\left(J_{\text{int}}+\delta-k\right)+\phi\right)} + \dfrac{\sin\left(\pi\left(J_{\text{int}}+\delta+k\right)\right)}{\sin\left(\dfrac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)} e^{-j\left(a\left(J+k\right)+\phi\right)} \right\} \\ +\sum_{h=2}^{H} \left(\begin{array}{l} \dfrac{b_h}{2M}\left\{ \dfrac{\sin\left(\pi\left(hJ_{\text{int}}+h\delta-k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)} e^{j\left(a\left(hJ_{\text{int}}+h\delta-k\right)+h\phi\right)} + \dfrac{\sin\left(\pi\left(hJ_{\text{int}}+h\delta+k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)} e^{-j\left(a\left(hJ_{\text{int}}+h\delta+k\right)+h\phi\right)} \right\} \\ -j\dfrac{a_h}{2M}\left\{ \dfrac{\sin\left(\pi\left(hJ_{\text{int}}+h\delta-k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)} e^{j\left(a\left(hJ_{\text{int}}+h\delta-k\right)+h\phi\right)} - \dfrac{\sin\left(\pi\left(hJ_{\text{int}}+h\delta+k\right)\right)}{\sin\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)} e^{-j\left(a\left(hJ_{\text{int}}+h\delta+k\right)+h\phi\right)} \right\} \end{array} \right) \end{array} \right) \tag{4.11}$$

From (4.11), it can be said that, the contribution from fundamental and harmonics on to other frequency bins is no longer zero due to the presence of non-integer δ. X_{Jint} not only contains the information of fundamental, but also contains the information of harmonics due to leakage. $2X_{Jint}$ not only contains the information of

second harmonic but also contains information of fundamental and other harmonics. Similarly, the power from each frequency component could leak into the surrounding bins. This leakage phenomenon is shown in Fig. 4.1 which is a spectrum of a non-coherently sampled data. Hence, the output of a non-coherently sampled data cannot be used directly to estimate the spectral characteristics.

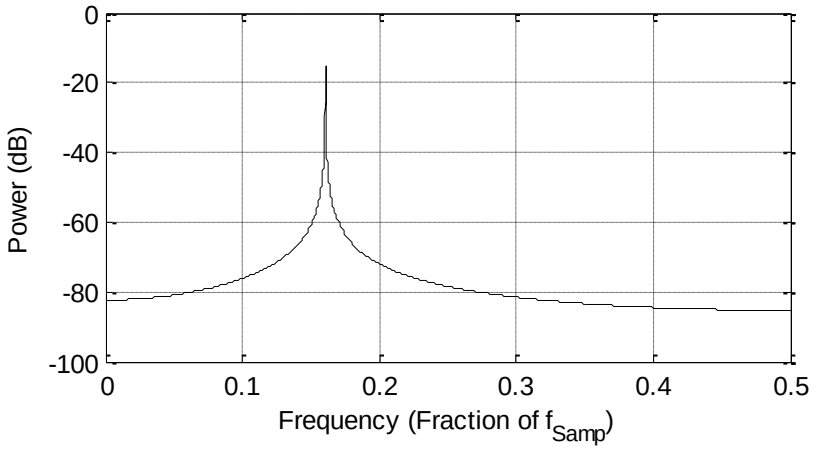

Figure 4.1: Power Spectrum of a non-coherently sampled data.

B) Impure (Non-linear) Signal Source

Another requirement to perform ADC spectral test is to acquire an input signal which is about 3 to 4 bits more pure than the ADC under Test. In this section, the issue with using non-linear input source to test high resolution ADC using conventional method is described.

If the input signal to the ADC under test is not a pure signal, *x(t)* is no longer a pure source as given by (4.2). The impure signal source $x_I(t)$ can be given by (4.12).

$$x_I(t) = A'\cos\left(2\pi f_{Sig} t\right) + \sum_{h=2}^{H} \alpha_{h0} \sin\left(2\pi h f_{Sig} t\right) + \beta_{h0} \cos\left(2\pi h f_{Sig} t\right) + w(t) \qquad (4.12)$$

where α_{h0} and β_{h0} contain the amplitude and phase information of h[th] harmonic present in input signal $x_I(t)$. The amplitude of fundamental component in $x_I(t)$ is given by A' so that the peak-to-peak voltage of $x_I(t)$ is within the input range of ADC under test. It can be seen that the notation used in equation (4.12) is similar to that used in equation (4.4) for convenience.

With impure signal source (given by $x_I(t)$) as input to the ADC under Test, the output of ADC, $x'[n]$, can be given as (4.13) [14].

$$x'[n] = \begin{pmatrix} A_1 \cos\left(\frac{2\pi J}{M} n + \phi\right) \\ +\sum_{h=2}^{H} (\beta_h + b_h)\cos\left(\frac{2\pi hJ}{M} n + h\phi\right) + (\alpha_h + a_h)\sin\left(\frac{2\pi hJ}{M} n + h\phi\right) + w[n] \end{pmatrix} \quad (4.13)$$

where A_1 is the amplitude of fundamental in ADC output $x'[n]$, $w[n]$ is noise in n[th] sampled point and α_h, β_h contain the amplitude and phase information of h[th] harmonic in input signal. α_h and β_h in (4.13) are dependent on the input impedance of ADC under test and on the values of α_{h0} and β_{h0}. If the input impedance of ADC under test is infinite, the values of α_h and β_h in (4.13) would be equal to the values of α_{h0} and β_{h0} in (4.12). a_h and b_h contain the amplitude and phase information of h[th] harmonic in ADC under test. To obtain the spectral characteristics of ADC, it is required to obtain the information of a_h and b_h.

Equation (4.13) is obtained after neglecting the higher order error terms that result from interaction between higher order harmonics (Eq. 6 in [14]). The validity of equation (4.13) is verified using simulation results. An input signal with harmonics as mentioned in equation (4.12) is generated in MATLAB. The values of α_{h0} and β_{h0} (for

each h) are noted. A 16-bit ADC with an INL of 1.5LSB and an input impedance of infinity is also generated. A total of 32768 points were considered for analysis and the SNR of the ADC was 94.2dB. A pure input signal that is coherently sampled is fed into the 16-bit ADC. The output of ADC using a pure source with coherent sampling is obtained and the values of a_h and b_h can be obtained from the DFT of ADC output as described in Chapter 1 (for standard testing). The values of a_h and b_h are noted down.

Later the same impure input (with the same values of α_{h0} and β_{h0}) is fed to the 16-bit ADC considered above. The output of ADC is coherently sampled and taking DFT gives the values of harmonics in the output of ADC. Let P_h and Q_h be the parameters that contain the information of amplitude and phase of hth harmonic in ADC output which is given by (4.14).

$$x'[n] = \begin{pmatrix} A_1 \cos\left(\frac{2\pi J}{M} n + \phi\right) \\ + \sum_{h=2}^{H} (P_h) \cos\left(\frac{2\pi hJ}{M} n + h\phi\right) + (Q_h) \sin\left(\frac{2\pi hJ}{M} n + h\phi\right) + w[n] \end{pmatrix} \tag{4.14}$$

It is assumed that the following two equations (4.15-4.16) are satisfied for the equation in (4.14) for each value of h from 2 to H. γ_h and ρ_h are the other terms in P_h and Q_h respectively that are due to the high order harmonic terms (considered negligible).

$$P_h = \beta_h + b_h + \gamma_h \tag{4.15}$$

$$Q_h = \alpha_h + a_h + \rho_h \tag{4.16}$$

Let γ, ρ and η be defined as vectors that are shown in equations (4.17 - 4.19).

$$\gamma = [\gamma_2 \quad \gamma_3 \quad . \quad . \quad . \quad \gamma_H] \tag{4.17}$$

$$\rho = \begin{bmatrix} \rho_2 & \rho_3 & . & . & . & \rho_H \end{bmatrix} \tag{4.18}$$

$$\eta = \begin{bmatrix} \gamma & \rho \end{bmatrix} \tag{4.19}$$

In (4.13), it is assumed that γ_h and ρ_h are negligible for all h (h = 2, 3, …, H). This assumption is validated by simulating 1000 runs in MATLAB. Fig. 4.2 plots the maximum value of η with respect to the SFDR of input signal for each run. It can be seen that the maximum values of η are in the range of 10^{-7} which is close to the noise floor of the ADC. As a result, it can be said that the assumption in equation (4.13) is valid and it can be used to model the output of ADC when an impure signal (about 10-bit pure) is fed into a high resolution ADC. Here input signal with SFDR about 60dB (or 10-bit pure) is considered as it is relatively easier to design (or procure) a signal generator that is about 10-bit pure.

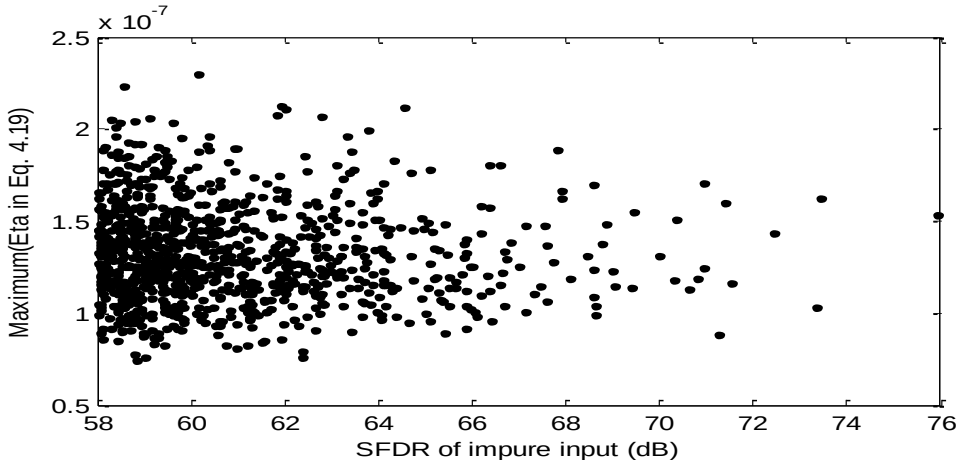

Figure 4.2: Figure plotting the maximum of η for each of the 1000 runs. It can be seen that the error is very small and is limited by the noise floor in the 16-bit ADC. Hence, with signals about 10-bit pure, Eq. 4.13 can be used for analysis.

Since the input signal is not pure than the ADC under test, it can be said that in equation (4.13) $\beta_h > b_h$ and $\alpha_h > a_h$. As a result, even if the sampling is coherent, taking

DFT of *x'[n]* in (4.13) would not result in accurate spectral results of ADC under test. The results obtained from DFT with coherent sampling would include the information of harmonics of both input and ADC under test. Hence, it is not possible to obtain the spectral characteristics of an ADC directly from DFT of output data if the input signal is not spectrally pure.

C) Non-coherent sampling and Impure Input Signal source

If an impure input that is non-coherently sampled is used to test a high resolution ADC, the spectrum obtained after taking DFT on the output of such ADC is shown in Fig. 4.3. It can be seen that the spectrum not only has leakage due to non-coherent sampling, but also has higher harmonics due to the non-linearity of the input signal. The spikes in the spectrum are due to the harmonics in the input signal and are not due to the harmonics in the ADC, as the input signal is less pure than the ADC under test. As a result, accurate spectral parameters cannot be estimated from the spectrum in Fig. 4.3. So, it is required to develop a new method that can accurately test high resolution ADCs using non-coherently sampled, non-linear input source to decrease the test cost.

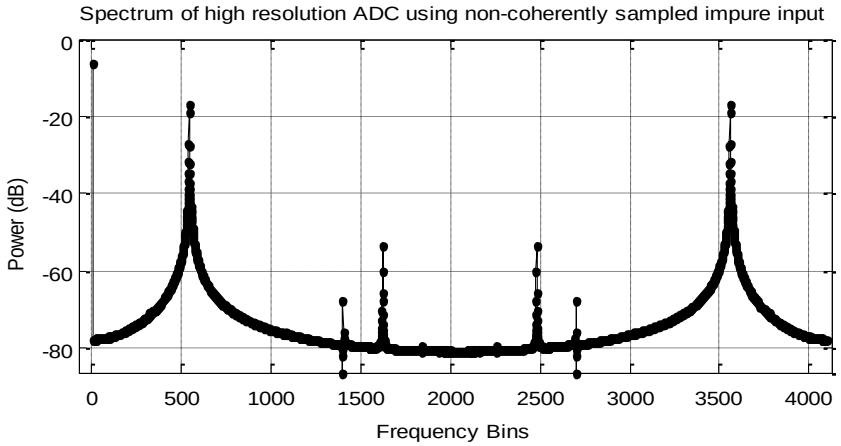

Figure 4.3: Spectrum of high resolution ADC with non-coherently sampled impure signal.

III. THE PROPOSED METHOD

The practical application of a production test setup using low cost testers is considered in this chapter as they do not have very pure signal sources. It is assumed that there is one signal source on the tester and different ADCs are tested at a fixed frequency and input range.

The test setup for the proposed method is shown in Fig. 4.4. The test is done in two steps. Step 0 is performed once and it characterizes the impure signal source with a very high resolution ADC, called Gold ADC. It should be made sure that the resolution of Gold ADC be greater than that of the ADC under test by at least 3 bits. The characterization of input source is done at a given frequency and input range. If there is any change in frequency or input range to be tested, step 0 needs to be repeated before starting to test the ADCs for the new frequency and input range.

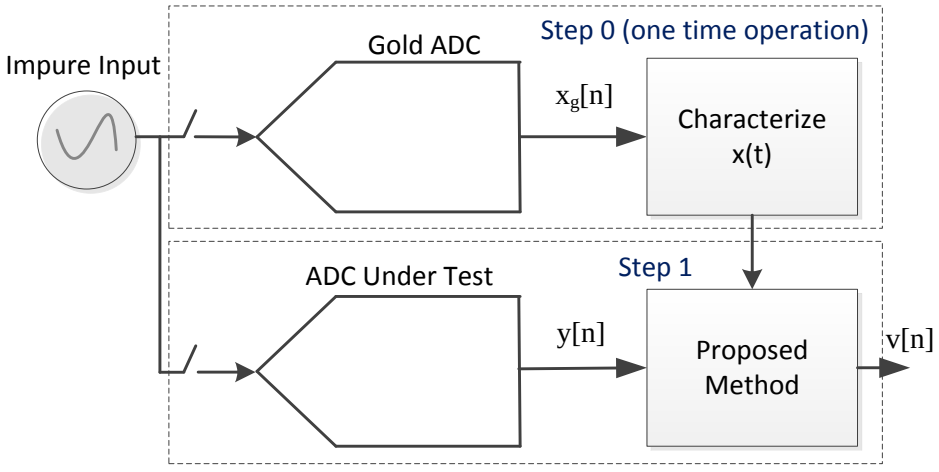

Figure 4.4: Test Setup for Proposed method

The regular production testing of ADCs is performed from Step 1. The information of impure source characterized in Step 0 is used to test high resolution ADCs in Step 1 using proposed method. The details of proposed method are presented below.

A) Step 0: Characterize the input Signal

In this section a method to characterize the non-coherently sampled input signal source is presented. The input signal not only contains fundamental but also contains harmonics as given by (4.12). The impure input signal is first fed into a Gold ADC and the output of Gold ADC is acquired and analyzed to accurately estimate the information of fundamental and harmonics of impure input signal.

Let $x_I(t)$ in (4.12) represent the impure signal that needs to be characterized. This is fed into Gold ADC. The amplitude of fundamental is selected such that the ADC output is not clipped. Let $x_g[n]$ in (4.20) represent the analog interpretation of digital output of Gold ADC when $x_I(t)$ in (4.12) is the input and after considering the first H harmonics. Since, the proposed method also aims at relaxing the condition of coherent sampling, J in (4.20) is not an integer. J can be given as the sum of J_{int} and δ as mentioned in Section IIA.

$$x_g[n] = \begin{pmatrix} A_1 \cos\left(\frac{2\pi J}{M} n + \phi\right) \\ + \sum_{h=2}^{H} \left(\beta_h + b_{g,h}\right) \cos\left(\frac{2\pi hJ}{M} n + h\phi\right) + \left(\alpha_h + a_{g,h}\right) \sin\left(\frac{2\pi hJ}{M} n + h\phi\right) + w[n] \end{pmatrix} \quad (4.20)$$

where A_1 is the fundamental amplitude in $x_g[n]$, α_h and β_h contain the amplitude and phase information of input signal's hth harmonic. $a_{g,h}$ and $b_{g,h}$ contain the amplitude and

phase information of Gold ADC's h[th] harmonic. As the input signal $x_I(t)$ is impure and the resolution of Gold ADC is about 3-4 bits more than that of the ADC under test, it can be said that $\beta_h >> b_{g,h}$ and $\alpha_h >> a_{g,h}$. As a result, the output of Gold ADC $x_g[n]$ can be given as (4.21).

$$x_g[n] = \begin{pmatrix} A_1 \cos\left(\frac{2\pi J}{M} n + \phi\right) \\ + \sum_{h=2}^{H} (\beta_h) \cos\left(\frac{2\pi hJ}{M} n + h\phi\right) + (\alpha_h) \sin\left(\frac{2\pi hJ}{M} n + h\phi\right) + w[n] \end{pmatrix} \quad (4.21)$$

From the output of Gold ADC given by (4.21), the input signal can be characterized by estimating A_1, J, ϕ, β_h and α_h (for h varying from 2 to H). The fundamental identification method proposed in chapter 2 cannot be used in this situation. It is because that method was based on the assumption that the power of harmonics is negligible. However, in (4.21), it can be seen that the harmonics are no longer negligible and a new method to identify all the parameters in (4.21) is required. A method to accurately identify all the above parameters using frequency domain data is provided.

1) Identify non-coherently sampled impure input signal (J_{int}, A_1, ϕ, δ, α_h, β_h)

First, the time domain data $x_g[n]$ is converted to frequency domain data using DFT on $x_g[n]$ to obtain $X_{g,k}$. $X_{g,k}$ in (4.22) corresponds to the DFT value of k[th] frequency bin.

$$X_{g,k} = \frac{1}{M} \sum_{n=0}^{M-1} x_g[n] e^{-j\frac{2\pi k}{M} n}, \text{ for } k = 0,1,2,\ldots,M-1 \quad (4.22)$$

From the DFT of $x_g[n]$, the value of J_{int} can be obtained by considering the frequency bin index that contains the maximum power in the spectrum excluding the bin corresponding to DC component (k=0). The mathematical equation for estimating J_{int} can be given as (4.23).

$$J_{\text{int}} = \arg\max_{1 \le k \le (M/2)} \left| X_{g,k} \right| \tag{4.23}$$

As J is not an integer, the value of $X_{g,k}$ after substituting (4.21) in (4.22) can be obtained as (4.24) after simplification.

From (4.24), $X_{g,k}$ can be given as sum of a real part and an imaginary part as shown in equation (4.25), where g_{rk} and g_{ik} are the real and imaginary parts of $X_{g,k}$ respectively. For k^{th} frequency bin, the values of g_{rk} and g_{ik} are given by equations (4.26-4.27) from (4.24).

The total number of parameters that need to be estimated from (4.21) is 2*H+1 (3 parameters δ, A_1 and ϕ for fundamental and 2 parameters β_h and α_h for h^{th} harmonic, h = 2, 3,…, H). From (4.26) and (4.27), it can be seen that both g_{rk} and g_{ik} are non-linear functions of J_{int} and δ. Since J_{int} is accurately estimated from (4.23), g_{rk} and g_{ik} are non-linear functions of δ. As a result, in order to accurately estimate all the parameters, Newton method for non-linear equations is used [16]. Since it is an iterative process, the initial values of all 2*H+1 parameters are required. The initial estimates of δ, A_1 and ϕ are obtained using equations (4.28-4.30) [17] from (4.22). The initial estimates of β_h and α_h (for all h = 2,3,..,H) are set to 1 as they are small.

$$X_{g,k} = \left(\begin{array}{l} \left(\begin{array}{l} \frac{A_1}{4} \left(\begin{array}{l} \left[\sin(2\pi\delta + \phi) - \sin(\phi) \right] \left(\begin{array}{l} \cot\left(\frac{\pi(J_{\text{int}} + \delta - k)}{M} \right) \\ + \cot\left(\frac{\pi(J_{\text{int}} + \delta + k)}{M} \right) \end{array} \right) \\ + 2\left[\cos(\phi) - \cos(2\pi\delta + \phi) \right] \end{array} \right) \\ + j \frac{A_1}{4} \left[\cos(\phi) - \cos(2\pi\delta + \phi) \right] \left(\begin{array}{l} \cot\left(\frac{\pi(J_{\text{int}} + \delta - k)}{M} \right) \\ - \cot\left(\frac{\pi(J_{\text{int}} + \delta + k)}{M} \right) \end{array} \right) \end{array} \right) \\ + \sum_{h=2}^{H} \left(\begin{array}{l} \frac{\beta_h}{4} \left(\begin{array}{l} \left(\begin{array}{l} \left[\sin(2\pi h\delta + h\phi) - \sin(h\phi) \right] \left(\begin{array}{l} \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta - k)}{M} \right) \\ + \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta + k)}{M} \right) \end{array} \right) \\ + 2\left[\cos(h\phi) - \cos(2\pi h\delta + h\phi) \right] \end{array} \right) \\ + j\left[\cos(h\phi) - \cos(2\pi h\delta + h\phi) \right] \left(\begin{array}{l} \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta - k)}{M} \right) \\ - \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta + k)}{M} \right) \end{array} \right) \end{array} \right) \\ + \frac{\alpha_h}{4} \left(\begin{array}{l} \left(\begin{array}{l} \left[\cos(h\phi) - \cos(2\pi h\delta + h\phi) \right] \left(\begin{array}{l} \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta - k)}{M} \right) \\ + \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta + k)}{M} \right) \end{array} \right) \\ - 2\left[\sin(2\pi h\delta + h\phi) - \sin(h\phi) \right] \end{array} \right) \\ - j\left[\sin(2\pi h\delta + h\phi) - \sin(h\phi) \right] \left(\begin{array}{l} \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta - k)}{M} \right) \\ - \cot\left(\frac{\pi(hJ_{\text{int}} + h\delta + k)}{M} \right) \end{array} \right) \end{array} \right) \end{array} \right) \end{array} \right) \end{array} \right) \quad (4.24)$$

$$X_{g,k} = \begin{pmatrix} g_{rk}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) \\ +jg_{ik}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) \end{pmatrix} \tag{4.25}$$

$$\begin{aligned} & g_{rk}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) \\ & = \frac{A_1}{4}\begin{pmatrix} \left[\sin\left(2\pi\delta+\phi\right)-\sin\left(\phi\right)\right]\left(\cot\left(\frac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)+\cot\left(\frac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)\right) \\ +2\left[\cos\left(\phi\right)-\cos\left(2\pi\delta+\phi\right)\right] \end{pmatrix} \\ & +\sum_{h=2}^{H}\begin{pmatrix} \frac{\beta_h}{4}\left(\begin{pmatrix} \left[\sin\left(2\pi h\delta+h\phi\right)-\sin\left(h\phi\right)\right]\left(\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\right. \\ \left.+\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\right) \\ +2\left[\cos\left(h\phi\right)-\cos\left(2\pi h\delta+h\phi\right)\right] \end{pmatrix}\right) \\ +\frac{\alpha_h}{4}\left(\begin{pmatrix} \left[\cos\left(h\phi\right)-\cos\left(2\pi h\delta+h\phi\right)\right]\left(\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\right. \\ \left.+\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\right) \\ -2\left[\sin\left(2\pi h\delta+h\phi\right)-\sin\left(h\phi\right)\right] \end{pmatrix}\right) \end{pmatrix} \end{aligned} \tag{4.26}$$

$$\begin{aligned} & g_{ik}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) \\ & = \frac{A_1}{4}\left[\cos\left(\phi\right)-\cos\left(2\pi\delta+\phi\right)\right]\left(\cot\left(\frac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)-\cot\left(\frac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)\right) \\ & +\sum_{h=2}^{H}\begin{pmatrix} \frac{\beta_h}{4}\left(\left[\cos\left(h\phi\right)-\cos\left(2\pi h\delta+h\phi\right)\right]\left(\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\right.\right. \\ \left.\left.-\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\right)\right) \\ -\frac{\alpha_h}{4}\left(\left[\sin\left(2\pi h\delta+h\phi\right)-\sin\left(h\phi\right)\right]\left(\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\right.\right. \\ \left.\left.-\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\right)\right) \end{pmatrix} \end{aligned} \tag{4.27}$$

$$\delta_0 = \frac{M}{2\pi} imag\left(\ln\left(\frac{\frac{X_{g,J_{\text{int}}}}{X_{g,J_{\text{int}}+1}} - \frac{X_{g,J_{\text{int}}}}{X_{g,J_{\text{int}}-1}}}{\frac{X_{g,J_{\text{int}}}}{X_{g,J_{\text{int}}+1}} - \frac{X_{g,J_{\text{int}}}}{X_{g,J_{\text{int}}-1}} + e^{j\frac{2\pi}{M}} - e^{-j\frac{2\pi}{M}}} \right) \right) \tag{4.28}$$

$$A_0 = 2M \left| X_{g,J_{\text{int}}} \right| \left| \frac{1 - e^{j\frac{2\pi\delta_0}{M}}}{1 - e^{j2\pi\delta_0}} \right| \tag{4.29}$$

$$\phi_0 = -imag\left(\ln\left(\frac{2MX_{g,J_{\text{int}}}}{A_0} \frac{1 - e^{j\frac{2\pi\delta_0}{M}}}{1 - e^{j2\pi\delta_0}} \right) \right) \tag{4.30}$$

Equations (4.28-4.30) are obtained after neglecting the effect of harmonics on $X_{g,Jint-1}$, $X_{g,Jint}$ and $X_{g,Jint+1}$. From equations (4.25-4.27), it can be seen that, two equations can be obtained for each value of k; one for real part and the other for imaginary part of $X_{g,k}$.

Let I be given as in (4.31) and $kSet$ in (4.32) contain values of frequency bin indices that are considered to obtain a set of equations to solve for 2*H+1 parameters.

$$I = J_{\text{int}} \tag{4.31}$$

$$kSet = \begin{Bmatrix} (I-1), (I), (I+1), (2I-1), (2I), (2I+1), (3I-1), \\ (3I), (3I+1), ..., (H*I-1), (H*I), (H*I+1) \end{Bmatrix} \tag{4.32}$$

A total of 3*H values of frequency bin indices (k) are selected in $kSet$ which results in a total of 6*H equations. The 6H equations considered are given in (4.33) as f_1, f_2, …, f_{6H}. Overall, a total of 6H equations can be considered to estimate the 2H+1 parameters.

$$
\begin{aligned}
f_1 &= g_{rJ_{\text{int}}-1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - real\left(X_{g,J_{\text{int}}-1}\right) = 0 \\
f_2 &= g_{iJ_{\text{int}}-1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - imag\left(X_{g,J_{\text{int}}-1}\right) = 0 \\
f_3 &= g_{rJ_{\text{int}}}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - real\left(X_{g,J_{\text{int}}}\right) = 0 \\
f_4 &= g_{iJ_{\text{int}}}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - imag\left(X_{g,J_{\text{int}}}\right) = 0 \\
f_5 &= g_{rJ_{\text{int}}+1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - real\left(X_{g,J_{\text{int}}+1}\right) = 0 \\
f_6 &= g_{iJ_{\text{int}}+1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - imag\left(X_{g,J_{\text{int}}+1}\right) = 0 \\
&\vdots \\
f_{6H-5} &= g_{rHJ_{\text{int}}-1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - real\left(X_{g,HJ_{\text{int}}-1}\right) = 0 \\
f_{6H-} &= g_{iHJ_{\text{int}}-1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - imag\left(X_{g,HJ_{\text{int}}-1}\right) = 0 \\
f_{6H-3} &= g_{rHJ_{\text{int}}}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - real\left(X_{g,HJ_{\text{int}}}\right) = 0 \\
f_{6H-2} &= g_{iHJ_{\text{int}}}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - imag\left(X_{g,HJ_{\text{int}}}\right) = 0 \\
f_{6H-1} &= g_{rHJ_{\text{int}}+1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - real\left(X_{g,HJ_{\text{int}}+1}\right) = 0 \\
f_{6H} &= g_{iJ_{\text{int}}+1}\left(A_1, J_{\text{int}}, \delta, \phi, \alpha_2, \beta_2, ..., \alpha_H, \beta_H\right) - imag\left(X_{g,HJ_{\text{int}}+1}\right) = 0
\end{aligned}
\tag{4.33}
$$

Let γ be the vector that contains all the parameters that needs to be estimated as shown in (4.34) and f be the vector containing the 6H equations as shown in (4.35). The size of γ is ((2H+1) x 1) and the size of f is (6H x 1).

$$\gamma = \begin{bmatrix} A_1 & \delta & \phi & \alpha_2 & \beta_2 & . & . & . & \alpha_H & \beta_H \end{bmatrix}^T \tag{4.34}$$

$$f = \begin{bmatrix} f_1 & f_2 & f_3 & . & . & . & f_{6H-2} & f_{6H-1} & f_{6H} \end{bmatrix}^T \tag{4.35}$$

To perform newton method, the Jacobean of f with respect to γ is required. Let *Jb* be the Jacobean which is given by (4.36). The size of *Jb* is (6H x (2H+1)). The equations to obtain the Jacobean matrix for given index k are given in Appendix.

$$Jb = \begin{bmatrix} \frac{\partial f_1}{\partial A_1} & \frac{\partial f_1}{\partial \delta} & \frac{\partial f_1}{\partial \phi} & \frac{\partial f_1}{\partial \alpha_2} & \frac{\partial f_1}{\partial \beta_2} & \cdot & \cdot & \frac{\partial f_1}{\partial \alpha_H} & \frac{\partial f_1}{\partial \beta_H} \\ \frac{\partial f_2}{\partial A_1} & \frac{\partial f_2}{\partial \delta} & \frac{\partial f_2}{\partial \phi} & \frac{\partial f_2}{\partial \alpha_2} & \frac{\partial f_2}{\partial \beta_2} & \cdot & \cdot & \frac{\partial f_2}{\partial \alpha_H} & \frac{\partial f_2}{\partial \beta_H} \\ \cdot & & & & & & & & \\ \cdot & & & & & & & & \\ \frac{\partial f_{6H-1}}{\partial A_1} & \frac{\partial f_{6H-1}}{\partial \delta} & \frac{\partial f_{6H-1}}{\partial \phi} & \frac{\partial f_{6H-1}}{\partial \alpha_2} & \frac{\partial f_{6H-1}}{\partial \beta_2} & \cdot & \cdot & \frac{\partial f_{6H-1}}{\partial \alpha_H} & \frac{\partial f_{6H-1}}{\partial \beta_H} \\ \frac{\partial f_{6H}}{\partial A_1} & \frac{\partial f_{6H}}{\partial \delta} & \frac{\partial f_{6H}}{\partial \phi} & \frac{\partial f_{6H}}{\partial \alpha_2} & \frac{\partial f_{6H}}{\partial \beta_2} & \cdot & \cdot & \frac{\partial f_{6H}}{\partial \alpha_H} & \frac{\partial f_{6H}}{\partial \beta_H} \end{bmatrix} \tag{4.36}$$

Let γ^i represent the values of parameters estimated in ith iteration, f^i be the vector of f (in 4.35) obtained by substituting the parameter values in ith iteration and Jb^i be the Jacobean matrix obtained by substituting the parameters obtained in ith iteration. For ith iteration, the value of γ^i is obtained using equation (4.37). The "\" operator is the least squares operator which performs on the Jacobean matrix, Jb and matrix of equations, f. The stopping criterion for the iterations can be either the total number of iterations (say 10) or the convergence of γ (such as $|\gamma^i-\gamma^{i-1}|<\varepsilon$).

$$\gamma^i = \gamma^{i-1} - Jb^{i-1} \setminus f^{i-1} \tag{4.37}$$

In other words, it can be mentioned that the newton method is applied to solve the following minimization problem given by (4.38) for γ.

$$\min_{\gamma} \| f \|_2^2 \tag{4.38}$$

With this, the final value of γ that contains the accurate estimates of A_1, ϕ, δ, α_2, β_2, …, α_H, β_H as $\widehat{A_1}, \widehat{\phi}, \widehat{\delta}, \widehat{\alpha_2}, \widehat{\beta_2}, \ldots, \widehat{\alpha_H}, \widehat{\beta_H}$ respectively are obtained. Hence, the non-coherently sampled impure input is characterized using Gold ADC.

B) Step 1: Testing the ADC (Device Under Test)

With the low-cost non-linear input characterized for a given amplitude and frequency in Step 0, the production test of ADCs can be performed in Step 1. It should be noted that Step 0 is only performed once.

Since the input to Gold ADC and the ADC under test are obtained from the same signal source, $x_I(t)$ in (4.12) is again considered as the input to ADC under test. Assuming the input impedance of ADC under test is the same as that of the Gold ADC, the output of ADC under test can be given as $y[n]$ in (4.39).

$$y[n]=\begin{pmatrix} A_1\cos\left(\frac{2\pi J}{M}n+\theta\right) \\ +\sum_{h=2}^{H}(\beta_h+b_h)\cos\left(\frac{2\pi hJ}{M}n+h\theta\right)+(\alpha_h+a_h)\sin\left(\frac{2\pi hJ}{M}n+h\theta\right)+w[n] \end{pmatrix} \quad (4.39)$$

where A_1 is the amplitude of fundamental in $y[n]$ and a_h and b_h contain the amplitude and phase information of hth harmonic of ADC under test. The values of α_h and β_h in equations (4.39) and (4.21) are the same as the input impedance of Gold ADC and ADC under test is same. θ is the initial phase at which the output of ADC ($y[n]$) is sampled.

To obtain the spectral characteristics of ADC, it is required to accurately estimate the information of harmonics of ADC (a_h and b_h in (4.39)). In (4.39), the contribution of harmonics from the impure input can be eliminated using the parameters estimated from Step 0 (α_h and β_h). However, it is required to estimate the initial phase θ in (4.39). To obtain accurate estimates, the procedure mentioned in Step 0 to identify the parameters is used on the output of ADC under test, $y[n]$. With this, the estimate of θ, ($\hat{\theta}$) in (4.39) is obtained. Using $\hat{\theta}$ and the parameters estimated in step 0, the contribution of non-

coherently sampled impure input in the output of ADC under test can be eliminated to get $z_y[n]$ as shown in (4.40-4.41).

$$z_y[n] = \begin{pmatrix} y[n] - A_1 \cos\left(\frac{2\pi J}{M} n + \hat{\theta}\right) \\ -\sum_{h=2}^{H}\left(\left(\beta_h\right)\cos\left(\frac{2\pi hJ}{M} n + h\hat{\theta}\right) + \left(\alpha_h\right)\sin\left(\frac{2\pi hJ}{M} n + h\hat{\theta}\right)\right) \end{pmatrix} \tag{4.40}$$

$$z_y[n] = \sum_{h=2}^{H}\left(\left(b_h\right)\cos\left(\frac{2\pi hJ}{M} n + h\theta\right) + \left(a_h\right)\sin\left(\frac{2\pi hJ}{M} n + h\theta\right)\right) \tag{4.41}$$

For each value of n in $z_y[n]$, the information of harmonics and noise at the codes hit by the ADC under test ($y[n]$) is obtained. But, this set of codes is not the same as the set of codes hit when using an ideal test signal that is pure and coherently sampled. To get the information of codes hit in an ideal test setup, a pure coherently sampled signal, $p[n]$, is generated using the information of A_1, J_{int} and θ as shown in (4.42).

$$p[n] = A_1 \cos\left(\frac{2\pi J_{\text{int}}}{M} n + \hat{\theta}\right) \tag{4.42}$$

It is required to get the information of harmonics and noise of ADC on the codes hit by $p[n]$. In order to obtain this information corresponding to each code in $p[n]$ (say $p[c]$), two codes in $y[n]$ that are near the code that is considered ($p[c]$) are used and interpolation of $z_y[n]$ at the two codes in $y[n]$ is performed. Fig. 4.5 provides an example for interpolation. In Fig. 4.5, y-axis represents the ADC codes that are hit and the x-axis represents the information of harmonics and noise of ADC at each code hit. The codes hit in $y[n]$ (x symbol in Fig. 4.5) are sorted and the corresponding values of $z_y[n]$ are plotted (+ symbol in Fig. 4.5). Similarly the codes hit in $p[n]$ (o symbol in Fig. 4.5) can

also be sorted on y-axis in Fig. 4.5. Let *p[c]* be the considered code for which the information of harmonics and noise, $z_p[c]$, needs to be estimated. As shown in Fig. 4.5, let *y[a]* and *y[b]* be the codes that were hit such that $y[b] < p[c] < y[a]$. Let $z_y[a]$ and $z_y[b]$ correspond to the information of harmonics and noise of ADC on codes hit by *y[a]* and *y[b]* respectively. The value of $z_p[c]$ (Δ symbol in Fig. 4.5) can be obtained by linear interpolation as given in equation (4.43).

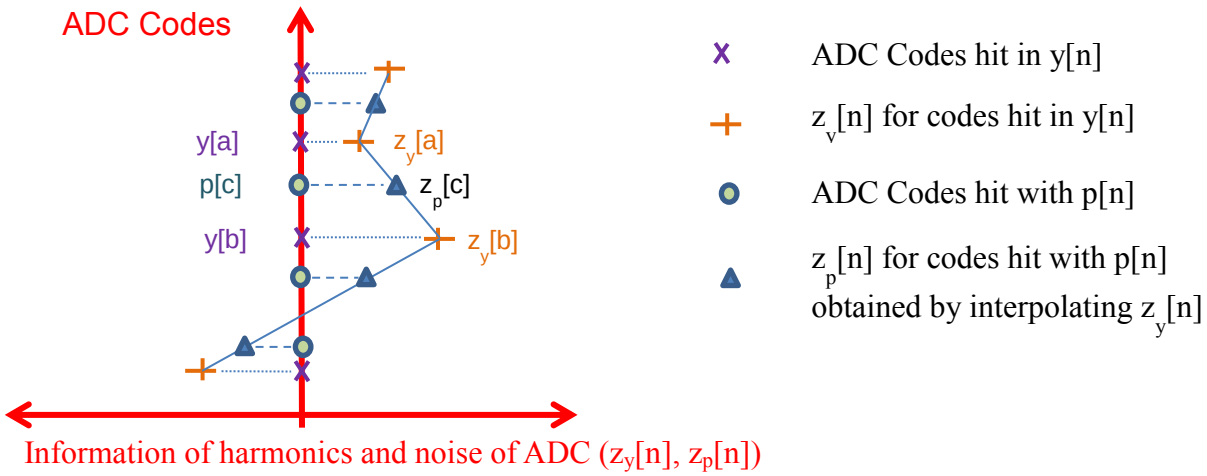

Figure 4.5: Figure illustrating the method of interpolating $z_y[n]$ to obtain $z_p[n]$

$$z_p[c] = z_y[a] + \frac{(z_y[b] - z_y[a])}{(y[b] - y[a])}(p[c] - y[a]) \tag{4.43}$$

After obtaining the information of harmonics and noise on each code hit by *p[n]*, this information is added to *p[n]* to obtain the final time domain output data given by *v[n]* as shown in (4.44).

$$v[n] = p[n] + z_p[n] \tag{4.44}$$

v[n] in (4.44) contains the fundamental and the information of harmonics and noise of ADC under test. Taking DFT of *v[n]* would result in estimating accurate

spectral characteristics of ADC under test as the fundamental in *v[n]* is coherently sampled and the information of input non-linearity is eliminated in *v[n]*.

IV. SIMULATION RESULTS

In this section, simulation results are presented that show the accurate functionality and robustness of the proposed method when a non-coherently sampled, impure input source is used to test a high resolution ADC.

A 15-bit ADC is generated in MATLAB with an INL of 1.6 LSB and a data record length, M of 4096. This ADC is the device under test. An input sine wave is generated from an oscillator circuit in cadence and the sine wave is used to test the device under test. The sine wave has an SFDR of 59dB. First, this sine wave is characterized using an 18-bit Gold ADC that is generated in MATLAB. The INL of Gold ADC is 1 LSB. After characterizing the input signal using Step 0, the same signal is used to test the 15-bit ADC under test. The spectrums obtained using the above test procedures are plotted in Fig. 4.6.

Fig. 4.6 shows three spectrum plots. The green spectrum is obtained by performing DFT on the 15-bit ADC output obtained after sending in the 59dB pure input. It can be seen that there is huge leakage in the spectrum as the signal is non-coherently sampled. The leakage in the spectrum is so large that it masked the harmonics of input signal. The blue spectrum is the spectrum of 15-bit ADC obtained using a pure coherently sampled input signal. It can be seen that there is no leakage and this spectrum is used as the reference to validate the proposed method. The 15-bit ADC output obtained after

feeding the 59dB pure non-coherently sampled input is processed using the proposed method and the spectrum obtained after processing is shown in Fig. 4.6 as the red plot. It can be seen that the red spectrum exactly matches with that of the blue spectrum. Table 4.1 provides the numerical values of spectral characteristics such as THD and SFDR obtained using the proposed method on non-coherently sampled, impure input and compares these characteristics with those obtained using standard method (coherent sampling + pure input). It can be said from Fig. 4.6 and Table 4.1 that the proposed method can accurately test the spectral characteristics of a high resolution ADC using a low linear (impure) source that is non-coherently sampled. Hence, two of the challenging conditions required to perform spectral testing are relaxed using the proposed method.

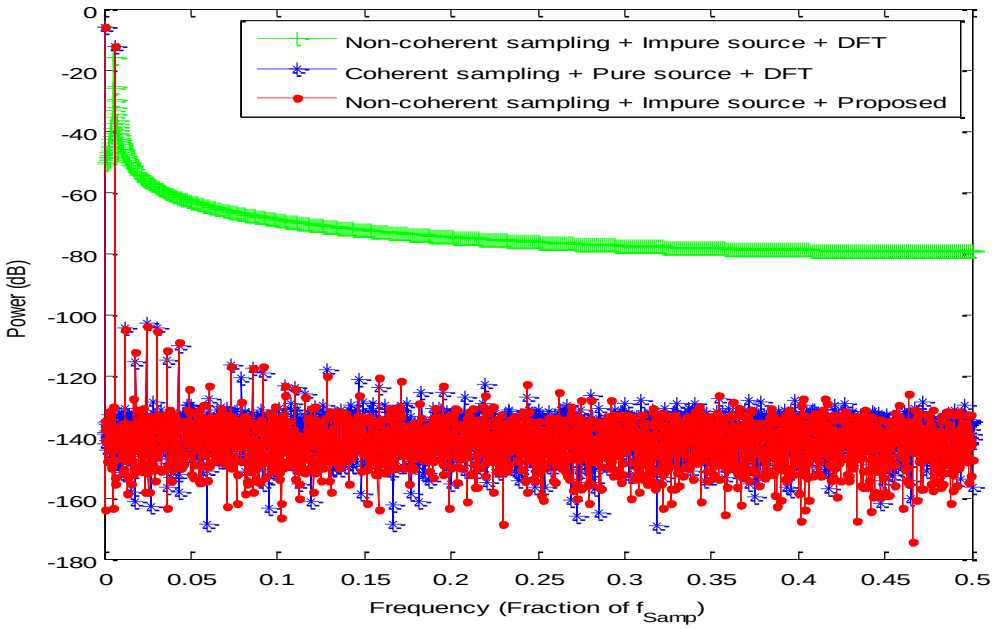

Figure 4.6: Spectrums of a 15-bit ADC with coherently sampled pure input (blue), non-coherently sampled impure input without (green) / with (red) using proposed method.

TABLE 4.1: Spectral characteristics of a 15-bit ADC tested with a Pure Source (Standard) and Impure + Non-coherent Source (Proposed)

Method	THD (dB)	SFDR (dB)
Coherent + Pure + DFT (Standard)	-86.3	90.8
Non-coherent + Impure + Proposed	-86.6	91.6

To examine the method proposed to characterize the input signal, an impure input signal with fundamental and odd harmonics is generated in MATLAB. An 18-bit Gold ADC with an INL of 0.85 LSB and infinite input impedance is also generated. The output of Gold ADC is acquired and the proposed method to characterize the input using Newton method for non-linear equations is used to estimate the values of α_h's and β_h's. Since the input signal is generated in MATLAB, the actual values of α_h's and β_h's are known. Table 4.2 provides the estimated values of α_h's and β_h's and the error in estimating these parameters. It can be seen that the method to characterize the input signal accurately estimates the required parameters. The SFDR of input source used is 39dB. Using this input and the proposed method, a 15-bit ADC with an INL of 2 LSB is tested for spectral characteristics. Fig. 4.7 shows the spectrums obtained for the three cases mentioned above. The reference case (coherent + pure source) is given by green spectrum, the DFT of ADC output is given by blue spectrum and the red spectrum is obtained after processing the ADC output using the proposed method. It can again be seen that the green and red spectrums match exactly and the spectral characteristics are accurately estimated using the proposed method as shown in Table 4.3.

TABLE 4.2: Estimation accuracy of input harmonics (in Step 0)

	Actual	Estimated	Error
α3	0	-8.10E-09	8.10E-09
β3	0.005003515	0.005003091	4.2E-07
α5	0	-2.50E-09	2.50E-09
β5	0.000648456	0.00064869	2.3E-07
α7	0	1.10E-08	1.10E-08
β7	0.000168798	0.000168709	8.9E-08
α9	0	2.50E-08	2.50E-08
β9	6.17718E-05	6.20273E-05	2.6E-07

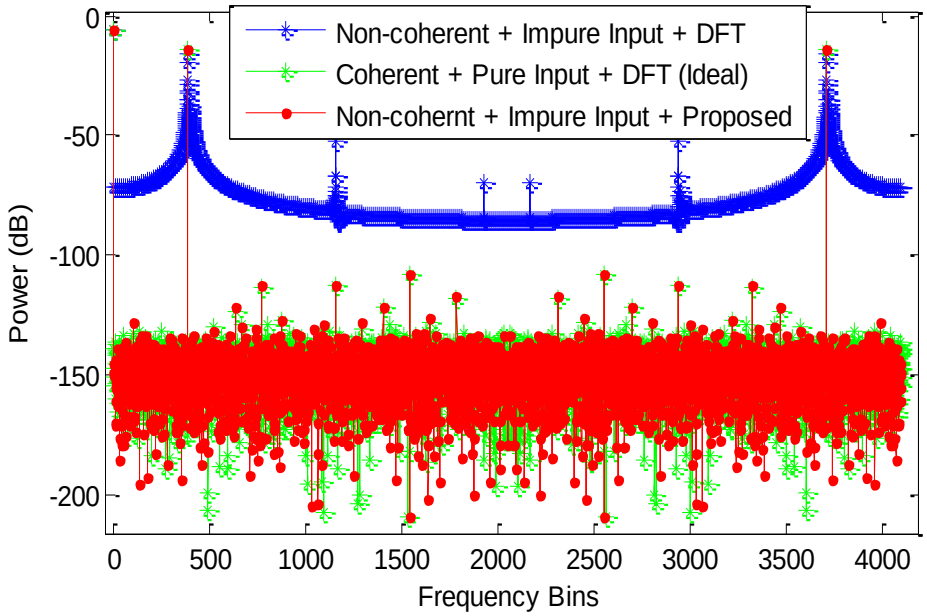

Figure 4.7: Spectrums of a 15-bit ADC with coherently sampled pure input (green), non-coherently sampled impure input without (blue) / with (red) using proposed method.

TABLE 4.3: Spectral characteristics of a 15-bit ADC tested with a Pure Source (Ideal) and Impure + Non-coherent Source (Proposed)

Method	THD (dB)	SFDR (dB)
Coherent + Pure + DFT (Standard)	-91.6	94.1
Non-coherent + Impure + Proposed	-91.2	94.0

The robustness of the proposed method with respect to the whole range of non-coherency ($\delta \in (-0.5\ 0.5]$) for 100 randomly selected δ values is shown in Fig. 4.8. The simulation conditions are the same as mentioned above. It can be seen that the error in estimating the THD and SFDR values is less than 1.5dB. As a result, the method is robust for any non-coherent sampling.

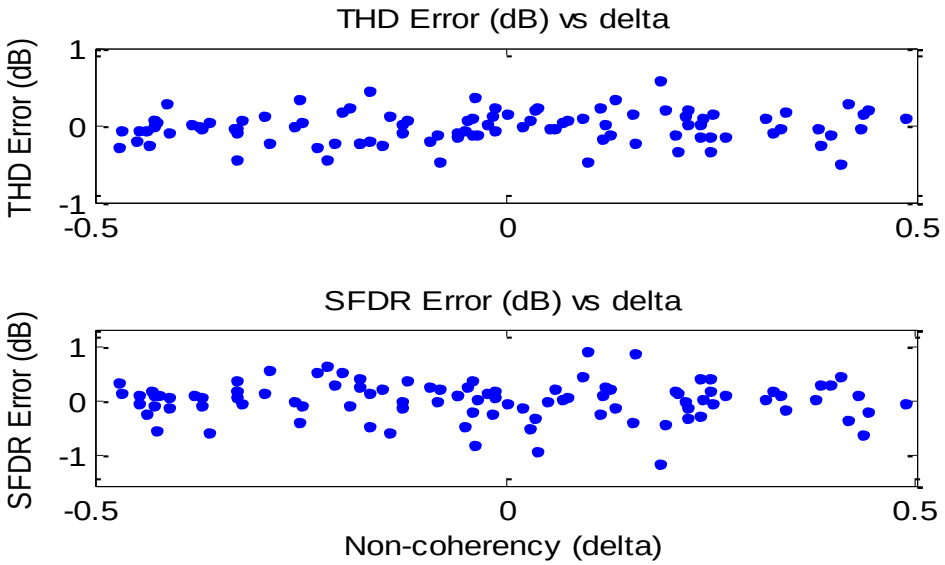

Figure 4.8: THD and SFDR errors for 100 randomly selected δ's in whole range (-0.5 0.5]

V. CONCLUSION

A new method was proposed that can accurately estimate the spectral characteristics of a high resolution ADC even when the input is impure and is non-

coherently sampled. The proposed method characterized the input source using a Gold ADC and then used this information of input source to test high resolution ADCs under test. A detailed explanation of the technique to accurately estimate all the parameters of the input signal was provided. Simulation results were presented that show accurate functionality and robustness of the proposed method. Two 15-bit ADCs were accurately tested using the proposed method with 39dB and 59dB pure input sources. The method decreases the test cost by reducing the cost associated with acquiring high linear sources and achieving coherent sampling.

VI. ACKNOWLEDGMENTS

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CHAPTER 5

ANALYSIS OF PROBABILITY OF METASTABILIY IN COMPARATORS AND SUCCESSIVE APPROXIMATION ADC

With increase in speed of analog electronics, the issue of metastability is starting to become a concern for comparators used in mixed signal circuits. In this chapter, a rigorous definition of metastability is proposed that can be used for any circuit exhibiting such behavior. The probability of metastability of two different comparator architectures is provided using mathematical analysis. It is shown that depending on the time at which the probability of metastability is evaluated, one comparator performs better than the other. Furthermore, mathematical analysis of probability of metastability is given for Successive approximation register Analog-to-Digital Converters with and without using metastable detection circuit. It is shown that as the frequency of sampling clock increases, the probability of metastability can be decreased by using a metastable detection circuit.

I. INTRODUCTION

Analog to Digital Converters (ADC) are one of the major building blocks of System on Chip (SoC) circuits. With developments in technology, there is an increase in the speed at which SoCs operate. As a result, it is required to design ADCs with higher clock speeds. However, with increase in ADC clock speed, one of the issues that arise is Metastability in comparators.

Metastability is a characteristic property of any system that contains either a comparator or a flip-flop. It is defined as the state in which the comparator does not provide a valid logic output. Typically, the output of comparator is connected to a digital circuit. For accurate operation of the digital circuit, the comparator output should be a valid logic "1" or logic "0". If the comparator is in a metastable state, the digital circuit does not function accurately as the input to the digital circuit is not a valid Boolean logic. Such cases could result in several problems such as system hang or improper operation [1]. As a result, it is very important to analyze the issue of metastability in a system and design accordingly.

The issue of metastability has been studied in the past. In [1], the observations of metastable behavior of flip-flops in response to logically undefined input conditions were shown. In [2], a first order model for a flip-flop was proposed to evaluate the probability of metastability. In [3-6], the effect of metastability in synchronizers or arbiters was presented. In [7, 8], techniques such as bit pipelining or cascading additional latches that increase the latency of ADC were proposed to tackle the issue of metastability in Flash ADCs.

In recent years, Successive Approximation Register (SAR) ADCs have been gaining a lot of interest due to their power efficiency and digital friendly architecture. In [9-11], different techniques to address the issue of metastability in Successive Approximation Register (SAR) ADCs were proposed one of which includes a Metastable-Then-Set (MTS) algorithm. Using MTS algorithm, the SAR operation is stopped as soon as a metastable output is detected, thus saving power in deciding the remaining bits. In [12], metastability in synchronous SAR ADC was explained and it was shown that metastability induced errors would become an important limitation in designing high speed SAR ADCs. An architecture for error correcting SAR ADC was presented that used a metastable detection circuit. However, analysis of probability of metastability after the error correction is used was not provided in [12].

In [5, 13], the output of the latch is connected to two inverters (Jamb latch) to reduce the failure rate. Appending inverters to the output of latch would increase the effective gain of the system and can help make a faster decision. However, an analysis that could determine when the technique is beneficial was not provided.

Though the issue of metastability was defined earlier as a phenomenon, it is required to have a rigorous mathematical definition for metastability in comparators. Such a definition could help analyze different techniques used for decreasing the probability of metastability and determine the parameters that contribute to metastability.

In this chapter, a rigorous mathematical definition for metastability in comparators is presented along with a method to determine the valid logic levels of the output of comparator. The probability of metastability of comparators with and without

appending an inverter is analyzed and situations when an inverter improves the probability of metastability are discussed. Furthermore, analysis of probability of metastability in synchronous SAR ADCs with and without using metastable detection circuit is provided.

The remaining of the chapter is arranged as follows. Section II provides the rigorous definition for metastability in circuits. Section III presents a method to determine the output voltages of comparator that corresponds to valid Boolean logic. Section IV analyzes the probability of metastability of a comparator with and without appending an inverter to the output of latch. Section V compares the probability of metastability of SAR ADC with and without using a metastable detection circuit. Section VI concludes the chapter.

II. METASTABILITY DEFINITION

Metastability is a characteristic property of any system that contains either a comparator or a flip-flop. Typically, the output of comparators is fed to a series of digital logic. For accurate functionality of the digital logic, it is required that the output of comparator provide a valid logic before the digital circuit is turned on. In other words, at the instance when the digital circuit is turned on, the output of comparator should be a valid logic 0 or logic 1. If the output of comparator at that instant is not a valid logic 0 or logic 1, the system is said to be metastable at that instance. Hence, metastability is a phenomenon that is defined at a given instant of time. A rigorous definition of metastable system is given below.

Metastable Definition: A system is said to be metastable at given time T_x, if there exists a time $T_1 > T_x$, such that

$$V_{LMAX} < V_{OUT}(T_1) < V_{HMIN} \tag{5.1}$$

where V_{LMAX} is the maximum voltage value that represents a valid logic "0", V_{HMIN} is the minimum voltage value that represents a valid logic "1" and $V_{OUT}(t)$ is the output voltage of the system at time "t" as shown in Fig. 5.1. It is considered that the comparator starts to compare at time t = 0.

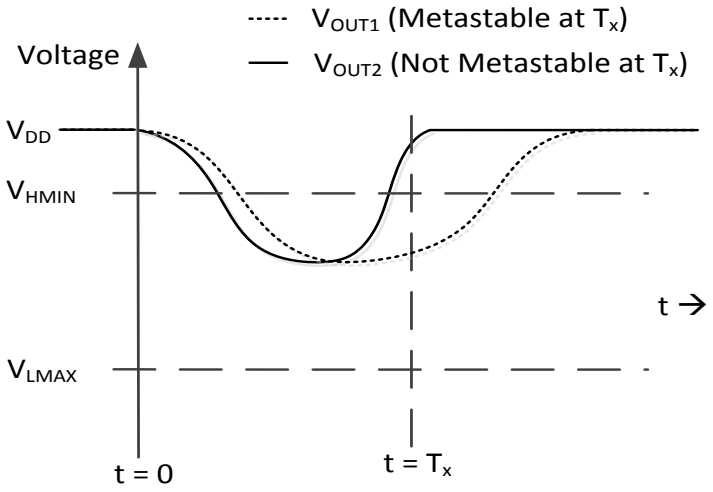

Figure 5.1: Figure illustrating the metastability phenomenon

The region of metastability, V_M, of a system at a given time T_x is the set of input voltage values that cause the system to be metastable. Pictorially, it can be represented as shown in Fig. 5.1. For any time instant after T_x, if the output waveform is within V_{LMAX} and V_{HMIN}, the event is metastable at time T_x. It can be seen from Fig. 5.1 that for input voltage V_{in2}, the output voltage waveform (V_{OUT2}) does not fall in the metastable

region and hence is not metastable at time T_x. However, for V_{in1}, the output waveform (V_{OUT1}) is within the metastable region and hence the system is metastable at time T_x.

Once the region of metastability, V_M, of a system at a given time T_x is known, the probability of metastability, P_{MS}, is obtained by taking the ratio of V_M to the total input range of the system.

Let V_{IN} be the input voltage of the system that ranges from $-V_R$ to $+V_R$. So, the total input range of the system is given as $2V_R$. With this, the probability of metastability of the system is given by (5.2).

$$P_{MS} = V_M/2V_R. \tag{5.2}$$

III. METHOD TO DETERMINE VALID LOGIC LEVELS

Having analytically defined the metastability, it is required to obtain the values of V_{HMIN} and V_{LMAX} in Fig. 5.1. Both the values are determined by the digital logic following the comparator. As a result, any output voltage value below V_{LMAX} is considered as logic 0 and any voltage value above V_{HMIN} is considered as logic 1 by the digital circuit. The following discussion provides a method to evaluate V_{LMAX} and V_{HMIN} in the simulation domain.

For simplicity, let us consider that the output of comparator is connected to a digital inverter. The first step in obtaining the values of V_{LMAX} and V_{HMIN} is to obtain the DC transfer characteristics of the inverter for all corners and different temperatures. Later the DC transfer curves using Monte-Carlo simulations including device

mismatches and process variations are obtained. The DC transfer curves for all the above simulations are plotted in a single plot as shown in Fig. 5.2. Fig. 5.2 shows the DC transfer curves of different process corners and two transfer curves obtained at the two extreme ends after performing Monte-Carlo simulations. From this plot, to find the trip point in each simulation, a line given by $V_{OUT} = V_{IN}$ is drawn. The trip point that corresponds to the maximum input voltage value is given as V_{HMIN} and the trip point that corresponds to the minimum input voltage is given as V_{LMAX} as shown in Fig. 5.2. This implies that for any input voltage of the inverter (output of comparator) greater than V_{HMIN}, the digital inverter considers it as a valid logic 1 and for any input voltage of the inverter less than V_{LMAX}, the digital inverter considers it as a valid logic 0. As a result, all process corners and mismatches were considered to obtain valid logic levels.

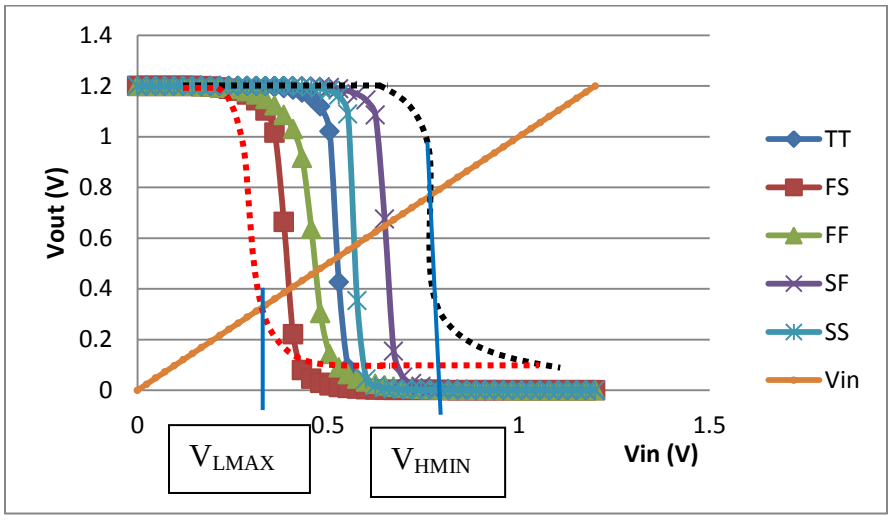

Figure 5.2: Transfer function curves for different corners and monte-carlo simulations of a digital inverter load (of comparator) to obtain the valid logic levels. Intersection of $V_{IN} = V_{OUT}$ line with the extreme ends of transfer curve gives the values of V_{HMIN} and V_{LMAX} (valid logic levels).

It should be noted that the procedure mentioned above is not limited to inverters but can also be used for any digital logic that is present after the comparator.

IV. PROBABILITY OF METASTABILITY OF COMPARATORS WITH AND WITHOUT ADDING INVERTERS

Having proposed a rigorous definition for metastability of comparators, the probability of metastability of a widely used comparator with and without appending inverters to the output of the latch is analyzed in this section.

The comparator that is considered is shown in Fig. 5.3. Let the comparator be called Comparator A. It consists of two NMOS input transistors M1 and M2 that amplify the input differential voltage, and a pair of back-to-back connected inverters that form a latch. The latch provides a positive pole and eventually pulls one output node to V_{DD} and the other output node to V_{SS} depending on the differential input to comparator. Two sets of switches (P2, P3 and P4, P5) are used to pre-charge the nodes V_{ON}, V_{OP}, V_A and V_B to V_{DD}. The load capacitance is given by C_L. If an inverter is connected as the load to the comparator, C_L is given by the input capacitance of the inverter. C_P is the parasitic capacitance on nodes V_A and V_B.

The operation of the comparator can be described in brief as follows. In the reset phase, clock CLK goes low, there by turning M7 off. During this phase, the switches P2-P5 are turned on, thus pulling nodes V_A, V_B, V_{OP} and V_{ON} to V_{DD}. In the comparison phase, clock CLK goes high. This turns on M7 and turns transistors P2-P5 off. If V_{IN} is larger than V_{REF}, node V_A is pulled down faster than that of node V_B. The regeneration

in latch (M3-M6) will eventually pull node V_{ON} down to V_{SS} and V_{OP} up to V_{DD}. Similarly, if V_{IN} is less than V_{REF}, V_{ON} is pulled up to V_{DD} and V_{OP} is pulled down to V_{SS}.

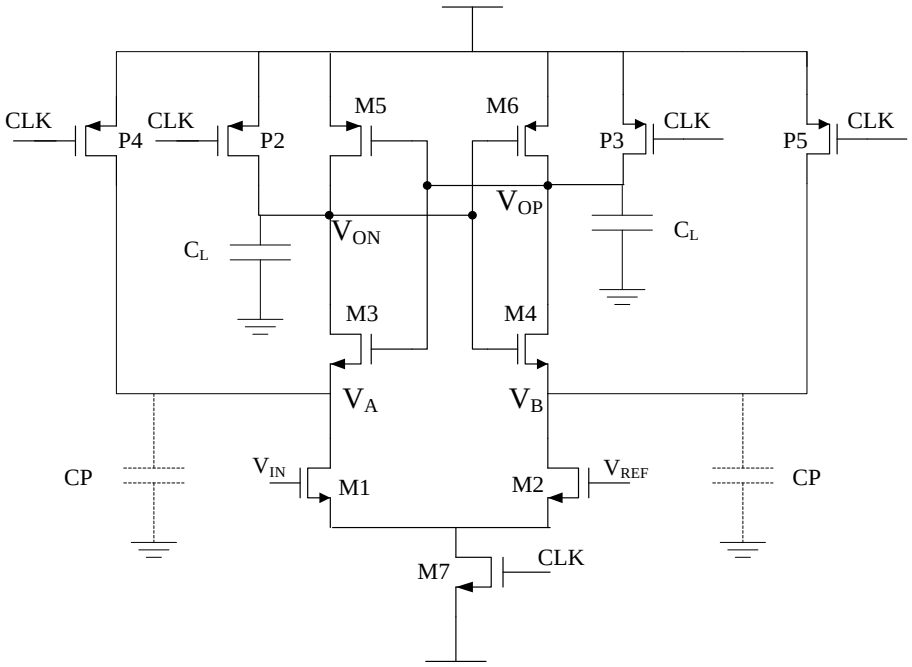

Figure 5.3: Schematic of Comparator A

It should be noted that each transistor in the comparator circuit changes the region of operation during comparison phase. In [14], the operation of comparator in comparison phase is separated into three states. State 1 corresponds to the state when CLK is just turned on. In this state, M7 is in triode region and M1, M2 are in saturation region while transistors M3-M6 are in cutoff region. The differential input voltage (V_{IN}-V_{REF}) is amplified to get differential output voltage (V_A-V_B). When node voltages of V_A and V_B are pulled down from V_{DD} to V_{DD}-V_{TN} (where V_{TN} is the threshold voltage of NMOS transistors), transistors M3, M4 enter saturation region. This corresponds to state

2, where transistors M1-M4 are in saturation, M5-M6 are in cutoff and M7 is in triode region. In this state, V_{OP} and V_{ON} start to fall from V_{DD}. When V_{OP} and V_{ON} are pulled to a voltage value V_{DD}-$|V_{TP}|$ (where V_{TP} is the threshold voltage of PMOS transistors), transistors M5, M6 are turned on and enter saturation. This corresponds to state 3 in which transistors M3-M6 are in saturation region, M1, M2 and M7 are in triode region. In this state, the regeneration takes place and will pull both the output nodes to opposite rails. It can be said that by the end of state 3, the decision would already be taken and further analysis is not required. In this comparator, the power is consumed only during comparison phase until the output nodes reach the rail, thus providing power efficiency.

A) Probability of Metastability of comparator (Comparator A)

When analyzing for the metastability of a comparator, the input voltage V_{IN} is considered to be very close to V_{REF}. In such cases, it can be said that the time taken to make a final decision is mainly dominated by state 3 compared to other two states. As a result, to perform further analysis of metastability, the equations of the comparator in state 3 are only considered. Also, the effect of offset is neglected to perform analysis in this chapter.

When analyzing comparator A in state 3, it can be seen that the four transistors (M3-M6) form a latch and the small signal output voltage, V_{OP} at time t, can be given as (5.3) [2, 14].

$$V_{OP}(t) = A_P (V_{IN} - V_{REF}) e^{\frac{t}{\tau_{L1}}} \tag{5.3}$$

where τ_{L1} is the regenerative time constant of the latch, A_P is the gain of the comparator, V_{IN} and V_{REF} are the input and reference voltages of comparator A respectively. τ_{L1} can be given as (5.4), where g_{mnL1} and g_{mpL1} are the trans-conductances of M3,M4 and M5,M6 respectively in state 3. In this analysis it is assumed that in state 3, the common mode voltage of the output of comparator stays constant and the small signal output voltage is given by (5.3). It is also assumed that the trans-conductance of transistors in saturation region is constant in each state of operation. From (5.3), the output voltage of comparator is dependent on input differential voltage, time constant of the latch and gain of the comparator. The speed of the comparator can be increased by either increasing the gain or differential input to the comparator or by decreasing the time constant of the comparator.

$$\tau_{L1} = \frac{C_L}{g_{mnL1} + g_{mpL1}} \tag{5.4}$$

In order to calculate the probability of metastability, it is first required to define an instant of time at which it needs to be calculated. Let t = 0 be the time instant when the clock CLK goes high to operate the comparator in comparison phase. Let t = T_P be the time instant at which the probability of metastability needs to be evaluated. After defining V_{HMIN} and V_{LMAX} from section III and neglecting time spent in states 1 and 2 compared to that spent in state 3, the region of metastability V_M can be obtained for comparator A using the definition of metastability provided in Section II.

The small signal output voltage, V_{OP} can reach either V_{DD} or V_{SS} depending on the input differential voltage. If input differential voltage is positive, that is, if V_{IN} is

greater than V_{REF}, the small signal output voltage would start from $A_P*(V_{IN}-V_{REF})$ at time t = 0 and ultimately reach V_{DD}. In this case, the maximum input voltage above V_{REF} that results in an output voltage of V_{HMIN} at time t = T_P can be given as V_{MH} in (5.5) using equation (5.3).

$$V_{MH} = V_{REF} + \frac{|V_{HMIN}|}{A_P} e^{-\frac{T_P}{\tau_{L1}}} \tag{5.5}$$

Similarly, the minimum input voltage below V_{REF} that results in an output voltage of V_{LMAX} at time t = T_P can be given as V_{ML} in (5.6).

$$V_{ML} = V_{REF} - \frac{|V_{LMAX}|}{A_P} e^{-\frac{T_P}{\tau_{L1}}} \tag{5.6}$$

So, the total region of metastability of comparator A can be given as $V_{M,A}$ in equation (5.7). Fig. 5.4 shows output waveforms of comparator A for different input voltages. It can be seen that for V_{IN} above V_{MH} or below V_{ML}, the comparator is not metastable at t = T_P. However, for input voltage V_{IN} within V_{ML} and V_{MH}, the comparator is metastable at t = T_P.

$$\begin{aligned} V_{M,A} &= V_{MH} - V_{ML} \\ V_{M,A} &= \frac{|V_{HMIN}| + |V_{LMAX}|}{A_P} e^{-\frac{T_P}{\tau_{L1}}} \end{aligned} \tag{5.7}$$

From (5.7), the probability of metastability of comparator A can be estimated by (5.8) as $P_{MS,A}$, where $2V_R$ is the total input range of V_{IN}.

$$P_{MS,A} = \frac{|V_{HMIN}| + |V_{LMAX}|}{2V_R A_P} e^{-\frac{T_P}{\tau_{L1}}} \tag{5.8}$$

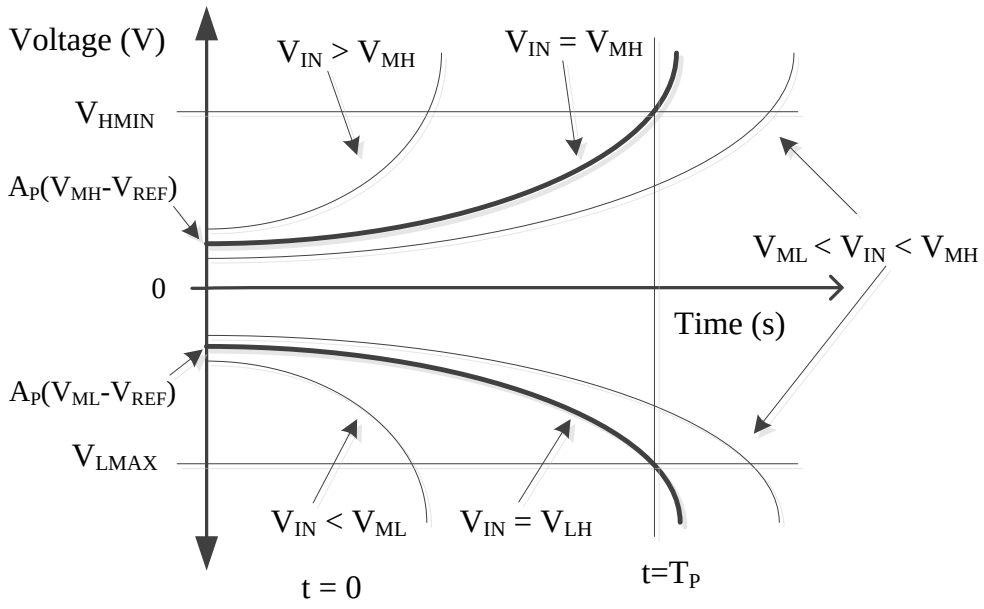

Figure 5.4: Plots showing the output voltage of comparator A for different input voltages around V_{REF}. Here $V_{MH} > V_{REF} > V_{ML}$. The thick lines correspond to maximum (V_{MH}) and minimum (V_{ML}) input voltages of comparator A that result in metastable output at t = T_P.

B) Probability of metastability of a comparator with inverters appended (Comparator B)

One of the techniques used to decrease the probability of metastability in comparators is to use inverters at the output of the latch as shown in Fig. 5.5 [5]. In Fig. 5.5, the comparator in Fig. 5.3 is appended with an inverter on both output nodes. Let the new comparator be called Comparator B. The output nodes of this comparator are V_{OIP} and V_{OIN} (output nodes of appended inverters). The load capacitance of comparator B is given by C_L. C_1 in Fig. 5.5 is the sum of parasitic capacitance on nodes V_{ON} (or V_{OP}) and input capacitance of the added inverters. Adding an inverter stage increases the overall

gain of comparator B and thus decreases the probability of metastability. The drawback with this method is that it adds slightly more power and introduces additional delay due to the inverter. The following description provides an analytical approach to determine the probability of metastability of comparator B and compare both comparators A and B.

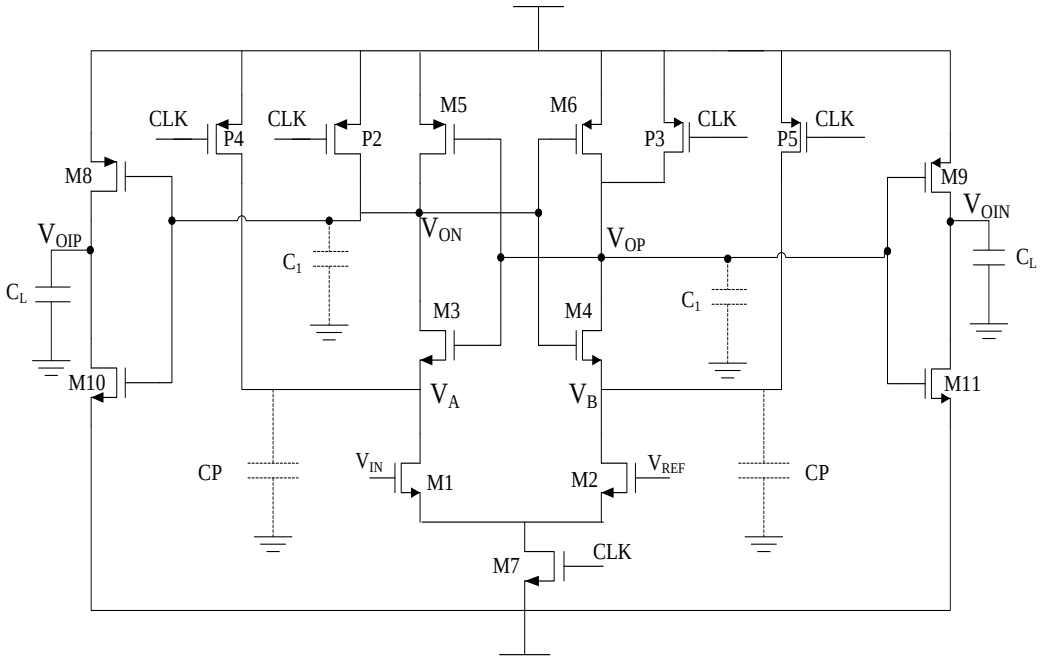

Figure 5.5: Schematic of comparator B

In Fig. 5.5, it is assumed that, the appended inverters are sized such that the trip point of inverters (M8-M11) is the same as that of the inverters present in the latch (M3-M6). It can be mentioned that when V_{IN} is close to V_{REF} the system is metastable and it can be assumed that all transistors in the latch (M3-M6) and in the inverters (M8-M11) are in saturation region. In this state, the small signal analysis can be performed for the above structure and the output voltage in s-domain can be given by (5.9). Equation (5.9)

is obtained by cascading a positive pole system (latch) with a negative pole system (inverter).

$$V_{OIP}(s) = \frac{A_{COMP}}{1 - s\tau_{L2}} \frac{A_{INV}}{1 + s\tau_{2I}} \frac{(V_{IN} - V_{REF})}{s} \tag{5.9}$$

where A_{COMP} is gain in the latch (M3-M6), A_{INV} is the gain of the appended inverter (M9,M11 or M8,M10), $1/\tau_{L2}$ and $1/\tau_{2I}$ are the magnitudes of positive and negative poles in the system at nodes V_{OP} (or V_{ON}) and V_{OIP} (or V_{OIN}) respectively. The values of A_{INV}, τ_{L2} and τ_{2I} can be given as (5.10-5.12).

$$A_{INV} = \frac{g_{mnI} + g_{mpI}}{g_{onI} + g_{opI}} \tag{5.10}$$

$$\tau_{L2} = \frac{C_1}{g_{mnL2} + g_{mpL2}} \tag{5.11}$$

$$\tau_{2I} = \frac{C_L}{g_{onI} + g_{opI}} \tag{5.12}$$

where g_{mnI} and g_{mpI} are the trans-conductances of the NMOS (M10-M11) and PMOS (M8-M9) transistors in the inverter respectively and g_{onI} and g_{opI} are the output conductances of NMOS and PMOS transistors in the inverters respectively, g_{mnL2} and g_{mpL2} are the trans-conductances of NMOS (M3-M4) and PMOS (M5-M6) transistors in the latch of comparator B respectively.

From (5.9), the small signal output voltage V_{OIP} in time domain can be given as (5.13). It can be noted that adding the inverter introduces a finite amount of delay which is given by t_{0INV} in (5.13).

$$V_{OIP}(t) = -A_{COMP}A_{INV}(V_{IN} - V_{REF})\left(\frac{e^{\frac{t-t_{0INV}}{\tau_{L2}}}}{1+\frac{\tau_{2I}}{\tau_{L2}}} + \frac{e^{-\frac{t-t_{0INV}}{\tau_{2I}}}}{1+\frac{\tau_{L2}}{\tau_{2I}}} - 1\right) \tag{5.13}$$

C_1 is usually small compared to that of C_L as the size of the inverter added to the output of latch in comparator B is usually smaller than the size of the digital circuit load to the comparator. Comparing τ_{L2} and τ_{2I}, it can be seen that since $C_L > C_1$ and $(g_{onI}+g_{opI}) < (g_{mnL2}+g_{mpL2})$, τ_{L2} is very small compared to τ_{2I}. Also, the second term in (5.13) is an exponential decay term with a time constant τ_{2I}. As a result, the second term in (5.13) can be neglected and the small signal output voltage of comparator B, V_{OIP} at time t can be given as (5.14) after neglecting the constant term.

$$V_{OIP}(t) = -\frac{A_{COMP}A_{INV}(V_{IN} - V_{REF})}{\left(1+\frac{\tau_{2I}}{\tau_{L2}}\right)}e^{\frac{t-t_{0INV}}{\tau_{L2}}} \tag{5.14}$$

Performing analysis similar to the one presented in the previous section and from (5.14), the region of metastability of comparator B at time T_P can be obtained as $V_{M,B}$ in (5.15)

$$V_{M,B} = \frac{(|V_{HMIN}| + |V_{LMAX}|)}{A_{COMP}A_{INV}}\left(1+\frac{\tau_{2I}}{\tau_{L2}}\right)e^{-\frac{T_P-t_{0INV}}{\tau_{L2}}} \tag{5.15}$$

The probability of metastability of comparator B at time t = T_P is given as $P_{MS,B}$ in (5.16)

$$P_{MS,B} = \frac{\left(|V_{HMIN}| + |V_{LMAX}|\right)}{2V_R A_{COMP} A_{INV}} \left(1 + \frac{\tau_{2I}}{\tau_{L2}}\right) e^{-\frac{T_P - t_{0INV}}{\tau_{L2}}} \tag{5.16}$$

C) Compare Probability of Metastability of comparator A and comparator B

Using equations (5.8) and (5.16), the probability of metastability of comparator A and comparator B is plotted in Fig. 5.6 with respect to the time at which it is evaluated, T_P. A total of four cases are plotted in which one case corresponds to comparator B while the other three cases correspond to comparator A. The values of A_P, A_{COMP} and A_{INV} are 6, 6 and 30 respectively; t_{0INV} was 150ps, while τ_{2I} and τ_{L2} are taken as 250ps and 58ps respectively. The value of $|V_{HMIN}|+|V_{LMAX}|$ is taken to be 1V.

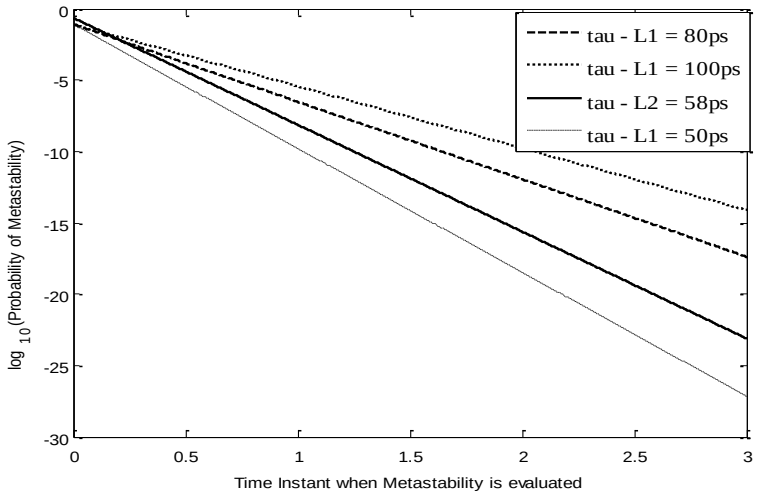

Figure 5.6: Probability of metastability of comparator B (solid line) and comparator A (dashed lines) for different values of τ_{L1}

The solid line in Fig. 5.6 represents the probability of metastability of comparator B with above mentioned values for varying T_P. The dashed lines in Fig. 5.6 represent the probability of metastability of comparator A for three values of τ_{L1} given by 50ps, 80ps and 100ps. The value of τ_{L1} can be changed by increasing or decreasing the g_{mnL1} and g_{mnP1} parameters (by changing the sizes of NMOS and PMOS transistors) as given in (5.4) for a given value of load capacitance (C_L). From Fig. 5.6, it can be said that, as τ_{L1} decreases, the probability of metastability also decreases in comparator A.

Now, comparing comparator A (dashed lines) and comparator B (solid line), two cases arise. Case 1 occurs when $\tau_{L1} < \tau_{L2}$, that is, comparator A is faster than the latch in comparator B. In such cases, the probability of metastability is always smaller for comparator A as shown in Fig. 5.6. Case 2 occurs when $\tau_{L1} > \tau_{L2}$, that is, comparator A is slower than the latch in comparator B. In such cases, it can be seen that there is a point in time (say T_P') until which comparator A has lower value of probability of metastability. After that point (T_P') in time, comparator B has lower probability of metastability. This phenomenon can be attributed to two factors in comparator B. Due to the delay produced by the additional inverter, t_{0INV}, the probability of metastability in comparator B at the beginning is more than that of comparator A. However, after some time (T_P'), the gain of the appended inverter along with the lower value of τ_{L2} would help decrease the probability of metastability of comparator B.

From equations (5.16) and (5.8), the value of T_P' is given by (5.17) and can be obtained by equating both $P_{MS,A}$ and $P_{MS,B}$.

$$T_P^{'} = \frac{\frac{t_{0INV}}{\tau_{L2}} + \ln\left(\frac{A_P}{A_{COMP}A_{INV}}\left(1+\frac{\tau_{2I}}{\tau_{L2}}\right)\right)}{\left(\frac{1}{\tau_{L2}} - \frac{1}{\tau_{L1}}\right)} \tag{5.17}$$

From the above analysis and from Fig. 5.6, it can be said that comparator A can be used if $\tau_{L1} < \tau_{L2}$ or if $\tau_{L1} > \tau_{L2}$ and T_P (time at which the probability of metastability is considered) is less than T_P'. If $\tau_{L1} > \tau_{L2}$ and T_P is greater than T_P', comparator B can be used to obtain lower probability of metastability.

V. PROBABILITY OF METASTABILITY OF SYNCHRONOUS SAR ADC WITH AND WITHOUT A METASTABLE DETECTION CIRCUIT

Another technique that is used to decrease the probability of metastability is to use metastable detection (MSD) circuit. The metastable detection circuits are used in systems that use comparators such as Analog-to-Digital converters. The probability of metastability in SAR ADCs with and without using MSD circuit is analyzed below.

A) SAR ADC without Metastable detection circuit

Let us consider a synchronous SAR ADC as shown in Fig. 5.7 with input range varying from $-V_R$ to V_R. A track and hold switch is present that samples the input voltage while the comparator, SAR logic and DAC perform the successive approximation operation to obtain the final digital output code.

1) SAR ADC Operation

Let N be the resolution of SAR ADC. φ_1 is the timing diagram of the sampling clock. Let T be the time period of sampling clock. Each period consists of two

phases, one is sampling phase and the other is conversion phase. Let T_S be the time allocated for sampling phase. In this phase, the analog input is sampled. In comparison phase, the digital output corresponding to the sampled input is obtained. Let T_D be the time period of internal clock $\varphi_{INTERNAL}$, within which a decision on one bit is made. As a result, the total time for comparison phase can be given as $N*T_D$. So, the sampling time period, T, can be given as the sum of time spent in sampling phase, T_S, and time spent in comparison phase, NT_D, as shown in equation (5.18).

$$T = T_S + NT_D \tag{5.18}$$

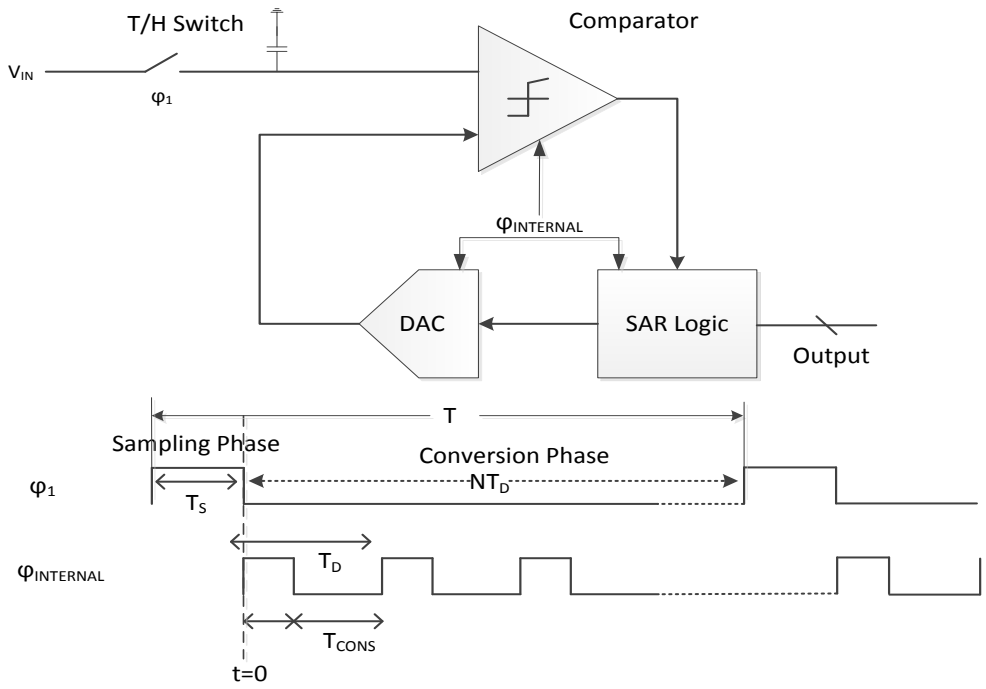

Figure 5.7: Block diagram of a successive approximation register (SAR) ADC with timing diagram

Let t = 0 correspond to the time at which the comparison phase starts as shown in Fig. 5.7. Using basic binary SAR operation, the decision on MSB (bit 1) is first made, then the decision on MSB-1(bit 2) is made and so on. To decide each bit, a total of

three operations need to be performed with in time period T_D. They are comparator decision, DAC settling and SAR logic operations. The time associated with DAC settling and SAR logic operation is constant. However, the time associated with comparator decision is not constant as the decision time is related to the input differential voltage as shown in equation (5.3). So, the maximum time available for comparator to make a decision is given as T_D-T_{CONS}, where T_{CONS} is the constant time allocated for DAC settling and SAR logic operation in determining one bit as shown in Fig. 5.7. A SAR ADC can deliver an accurate output if the comparator provides a valid output within time $T_D - T_{CONS}$.

2) Probability of Metastability in SAR ADC

In SAR ADC, the probability of metastability is given by the regions of metastability that is occurred when deciding each bit. The comparators used in SAR ADC are similar to the ones discussed in Section IV above. Hence, similar equations are used to estimate the probability of metastability in SAR ADCs.

From (5.7), the region of metastability when the first bit (MSB) is decided is given as V_{M1} as shown in (5.19). This is because there is only one possible reference voltage with which the input is compared to determine MSB bit in SAR operation. Here τ_1 and A are the time constant and gain of comparator in Fig. 5.7 respectively and ($T_D - T_{CONS}$) is the total time available for the comparator in Fig. 5.7 to make a valid decision. As explained in Section III, V_{HMIN} and V_{LMAX} can be obtained from the digital circuitry in SAR logic.

$$V_{M1} = \frac{|V_{HMIN}| + |V_{LMAX}|}{A} e^{-\frac{T_D - T_{CONS}}{\tau_1}} \tag{5.19}$$

To determine the second bit, there are two possible reference voltages ($V_{REF}/4$, $3V_{REF}/4$). As a result, the region of metastability for second bit decision is given as V_{M2} and is shown in (5.20). V_{M2} is two times V_{M1} as there are two possible reference voltages.

$$V_{M2} = 2\frac{|V_{HMIN}| + |V_{LMAX}|}{A} e^{-\frac{T_D - T_{CONS}}{\tau_1}} \tag{5.20}$$

Similarly, to determine i^{th} bit (bit 1 is MSB and bit N is LSB), there are a total of $2^{(i-1)}$ possible reference voltages. As a result, the region of metastability to determine i^{th} bit is given as V_{Mi} and is shown in (5.21).

$$V_{Mi} = 2^{i-1}\frac{|V_{HMIN}| + |V_{LMAX}|}{A} e^{-\frac{T_D - T_{CONS}}{\tau_1}} \tag{5.21}$$

So, the total region of metastability for a SAR ADC can be given as $V_{M,ADC}$ in equation (5.22). From $V_{M,ADC}$, the probability of metastability of SAR ADC without a metastable detector can be given as $P_{MS,ADC}$ in (5.23).

$$V_{M,ADC} = \sum_{i=1}^{N} V_{Mi} = \left(2^N - 1\right)\frac{|V_{HMIN}| + |V_{LMAX}|}{A} e^{-\frac{T_D - T_{CONS}}{\tau_1}} \tag{5.22}$$

$$P_{MS,ADC} = \frac{V_{M,ADC}}{2V_R} = \left(2^N - 1\right)\frac{|V_{HMIN}| + |V_{LMAX}|}{2V_R A} e^{-\frac{T_D - T_{CONS}}{\tau_1}} \tag{5.23}$$

B) SAR ADC with Metastable detection circuit

Now consider SAR ADC architecture as shown in Fig. 5.8 with input range varying from $-V_R$ to V_R. It can be seen that a metastable detection circuit and an error correction block are added to the SAR ADC in Fig. 5.7 and the timing diagram for the operation of this new SAR ADC is provided in Fig. 5.8. The functioning of SAR logic, DAC and comparator 1 in Fig. 5.8 is similar to the one in Fig. 5.7. As a result, the timing diagrams for clocks φ_1 and $\varphi_{INTERNAL}$ are the same in both Fig. 5.7 and Fig. 5.8. The other timing diagrams of φ_M and φ_{EC} correspond to the metastable detection (MSD) circuit and error correction block.

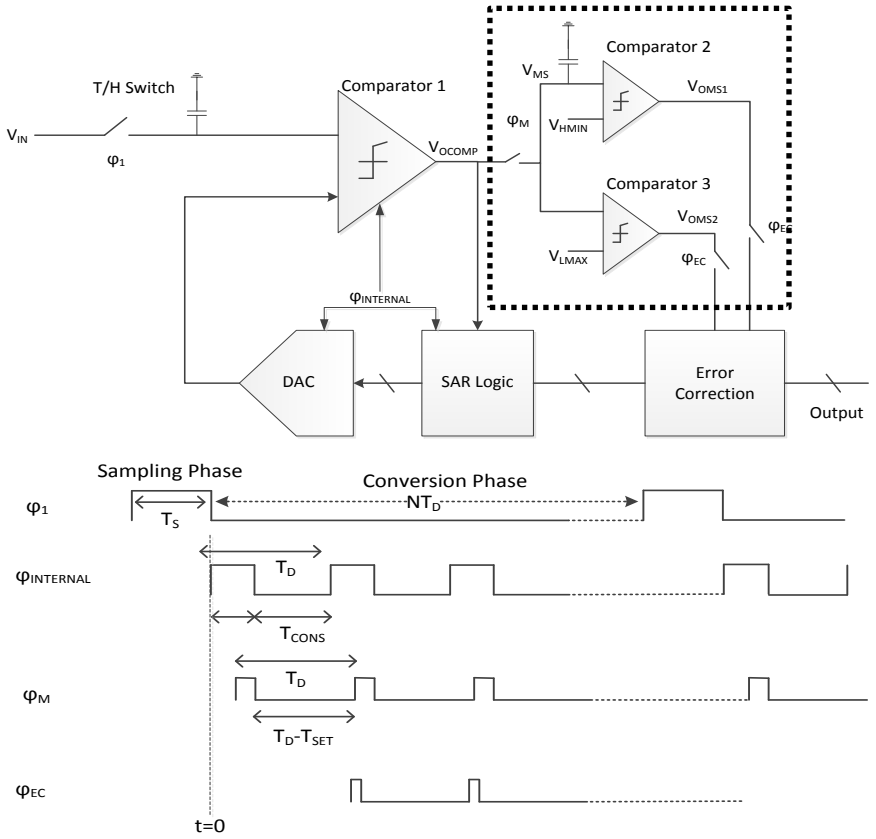

Figure 5.8: Block diagram of a successive approximation SAR ADC with a metastable detection circuit and error correction block. Timing diagram of different clocks used is given.

1) Operation of the Metastable detection (MSD) circuit

The metastable detection (MSD) circuit includes a track and hold switch, one comparator (comparator 2) with trip voltage V_{HMIN} and another comparator (comparator 3) with trip voltage V_{LMAX} as shown in Fig. 5.8. The MSD circuit holds the output voltage of comparator 1 at a given instant and checks if comparator 1 is metastable or not. Ideally, a metastable event is detected if the voltage value on node V_{MS} is between V_{HMIN} and V_{LMAX}. If the voltage value on node V_{MS} is not in between V_{HMIN} and V_{LMAX}, comparator 1 is not metastable when deciding that particular bit. When φ_M goes high, node V_{OCOMP} is tracked and when φ_M goes low, the voltage value on node V_{OCOMP} is held on node V_{MS} using the track and hold circuit. In the MSD circuit, if the outputs of both comparators (comparator 2 and comparator 3) are either logic "0" or logic "1", a metastable event is not obtained. However, if output of comparator 2 is logic "0" and output of comparator 3 is logic "1", a metastable event is said to be detected.

2) Functioning of Error Correction Block

The error correction block functions based on the outputs of SAR logic and the metastable detection circuit. If MSD circuit does not detect a metastable event, the output of error correction block would be the same as the output of SAR logic in Fig. 5.8. However, if the MSD detects a metastable event, the error correction block produces an output code depending on the bit at which the metastable event is detected. For example, if the MSD circuit detects a metastable event when deciding the i^{th} bit, the error correction block provides an output such that the first (i-1) bits (from bit 1 (MSB) to bit (i-1)) are retained from the output of SAR logic, then it fixes the i^{th} bit to 1 and the

following bits (bit i+1 to bit N (LSB)) to 0 (similar to MTS algorithm [11]). As a result, the metastable event is detected and is corrected in the output of ADC. Clock φ_{EC} is used to fetch the output of comparators in MSD circuit to perform error correction.

3) SAR ADC Functionality

Having described the operation of MSD circuit and error correction, the overall functionality of the SAR ADC using a MSD circuit is explained below.

Once the analog input voltage is sampled and settled by the end of sampling phase, the conversion phase starts. Let t = 0 correspond to the time at which the conversion phase starts for each sample as shown in Fig. 5.8. For proper operation of the DAC and SAR logic, comparator 1 should provide a valid logic output by time $t = T_D - T_{CONS}$. This output voltage is held on node V_{MS} using a clock φ_M with a pulse width of T_{SET} and a period of T_D. Ideally, the comparators in MSD circuit compare the voltage value on node V_{MS} with V_{HMIN} and V_{LMAX} and output accordingly. Both the comparators in the metastable detection circuit should provide a valid logic output within time $T_D - T_{SET}$. Since the comparators in MSD circuit starts to operate from time $t = T_D - T_{CONS}$, a valid output from comparator 2 and comparator 3 should be obtained by time $t = T_D - T_{CONS} + T_D - T_{SET}$. This is the time when the error correction block fetches the output of MSD circuit and performs correction if required and provides the output of SAR ADC.

As mentioned above if a metastable event is not detected, the SAR logic output is considered as the output of ADC and if a metastable event is detected, the error correction block corrects the output of SAR logic and provides accurate output of ADC. It can be seen that the MSD circuit added in Fig. 5.8 does not fall in the signal path for

SAR operation. As a result, the output of SAR ADC in Fig. 5.8 is obtained with latency, but the frequency of the sampling clock is still the same as used in Fig. 5.7. Hence, the effects of metastability in SAR ADC at a given frequency can be decreased using a metastable detection circuit by detecting and correcting a metastable event

4) Probability of Metastability using Metastable detection circuit

In the SAR ADC shown in Fig. 5.8, though a MSD circuit is used, there is some probability of metastability still present due to the fact that both comparators included in the metastable detection circuit are susceptible to metastability. The comparator with reference voltage equal to V_{HMIN} (comparator 2) could be metastable if voltage held on node V_{MS} is close to V_{HMIN} and similarly the comparator with reference voltage equal to V_{LMAX} (comparator 3) could be metastable when voltage held on node V_{MS} is close to V_{LMAX}. Hence, it is required to find the probability of metastability of SAR ADC when a metastable detection circuit is used. The probability of metastability in SAR ADC with metastable detection circuit as shown in Fig. 5.8 is explained below using Fig. 5.9.

The region of metastability of the SAR ADC in Fig. 5.8 when deciding the MSB bit (bit 1) is explained in Fig. 5.9. The reference voltage of comparator 1 considered in Fig. 5.9 is zero (for MSB bit). In this explanation, MSB bit decision is chosen for convenience. The same explanation holds good when deciding any bit.

There are two different graphs present in Fig. 5.9. The graph to the left corresponds to the output voltage in comparator 1 with reference voltage, $V_{REF} = 0$ (considering MSB bit). The graph to the right (red **bold**) corresponds to the output

voltage of comparator 2 with reference voltage $V_{REF} = V_{HMIN}$. The output voltage of comparator 1is plotted from t = 0 to t = $T_D - T_{CONS}$ in the left part of Fig. 5.9. The output voltage of comparator 2 is plotted from t = $T_D - T_{CONS}$ to t = $T_D - T_{CONS} + T_D - T_{SET}$ in the right part of Fig. 5.9. As mentioned earlier, the output voltage of comparator 2 at t = $T_D - T_{CONS} + T_D - T_{SET}$ is fetched by error correction block.

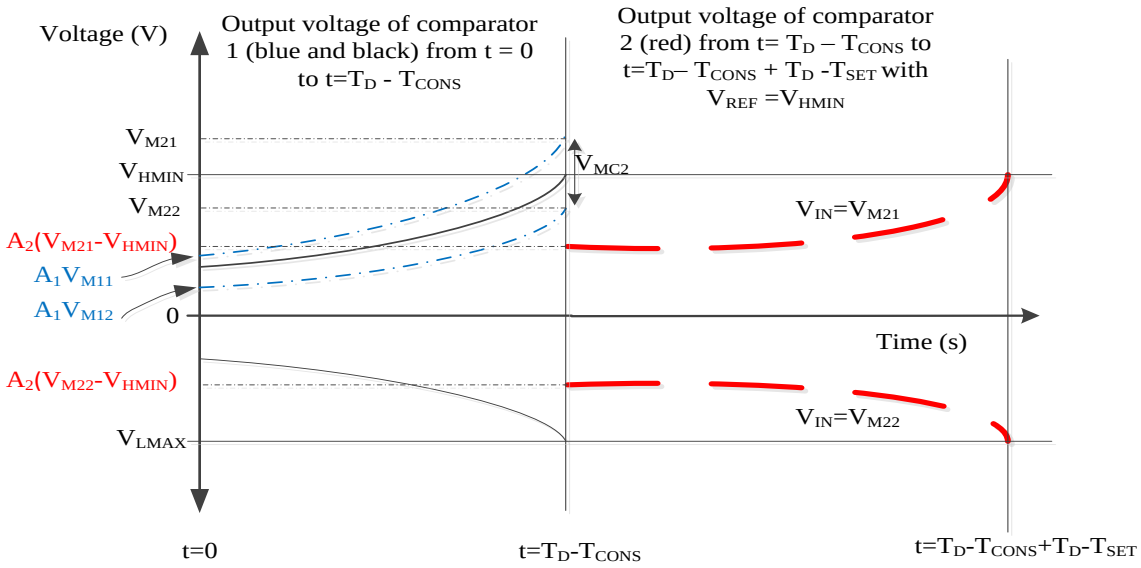

Figure 5.9: Output voltages of comparator 1 and comparator 2 plotted on the same time and voltage axis. Left part is the output voltage of comparator 1 (Blue-dashed curves), right part is the output voltage of comparator 2 (red-dashed). VMC2 is the region of metastability of comparator 2 around VHMIN. VM11 and VM12 are the maximum and minimum input voltages of comparator 1 that result in an output of comparator 1 to fall in the range of VMC2, thus causing comparator 2 to be metastable.

First, considering the graph on right side of Fig. 5.9, the region of metastability of comparator 2 around V_{HMIN} is obtained. This is shown in Fig. 5.9 as ($V_{M21} - V_{M22}$) or V_{MC2} using the blue-dashed curves at time t = T_D - T_{CONS}. V_{MC2} corresponds to the range of input voltages around V_{HMIN} that results in a metastable output for comparator 2 at time t = $T_D - T_{CONS} + T_D - T_{SET}$ (red curves in Fig. 5.9). The

top red-dashed curve is the output of comparator 2 with input voltage V_{M21}, while the bottom red curve is the output of comparator 2 with input voltage V_{M22}. A_2 is the gain of comparator 2 and comparator 3.

It can be seen from Fig. 5.8 that, the input to comparator 2 is the output of comparator 1. As a result, from the range of metastability of comparator 2 (which is given as $V_{M21} - V_{M22}$), the set of input voltages to comparator 1 that result in an output to fall in the range of [V_{M22} V_{M21}] at $t = T_D - T_{CONS}$ can be obtained (by tracing the blue dashed lines backwards). In left graph of Fig. 5.9, the top blue-dashed curve is the output of comparator 1 with input voltage V_{M11} (gives output voltage V_{M21} at $t = T_D - T_{CONS}$) and the bottom blue-dashed curve is the output of comparator 1 with input voltage V_{M12} (gives output voltage V_{M22} at $t = T_D - T_{CONS}$). As a result, the range of input values to comparator 1 that produce a metastable event in comparator 2 is given by V_{M11}-V_{M12}. A_1 is the gain of comparator 1 in Fig. 5.8. Similarly, the range of input voltages that result in comparator 3 to enter metastability can be obtained. The analysis to achieve the probability of metastability depending on different comparator parameters is given below.

Considering the same comparator circuit as discussed in Section IV (comparator A), the output voltage of comparator 1 in Fig. 5.8, V_{OCOMP}, at time t with input V_{IN} and reference voltage, $V_{REF} = 0$ (considering MSB bit decision), can be given as (5.24). Here τ_{21} is the time constant of comparator 1.

$$V_{OCOMP}(t) = (V_{IN} - 0) A_1 e^{\frac{t}{\tau_{21}}} \tag{5.24}$$

The voltage on node V_{OCOMP} at time $t = T_D - T_{CONS}$ is held on node V_{MS} to detect metastable event. As mentioned above, V_{M11} is the input voltage to comparator 1 that results in an output voltage V_{M21} at time $t = T_D - T_{CONS}$. From (5.24), V_{M21} can be given as (5.25).

$$V_{M21} = (V_{M11} - 0) A_1 e^{\frac{T_D - T_{CONS}}{\tau_{21}}} \tag{5.25}$$

It is also known that V_{M21} is the input voltage of comparator 2 that is greater than V_{HMIN} and provides an output voltage of comparator 2 equal to V_{HMIN} at time $t = T_D - T_{CONS} + T_D - T_{SET}$ from Fig. 5.9. The output voltage of comparator 2 at $t = T_D - T_{CONS} + T_D - T_{SET}$ can be given as (5.26) from (5.3). Here τ_{22} is the time constant of comparator 2, T_D-T_{SET} is the total time available for comparator 2 to make a decision and V_{OMS1} is the output voltage of comparator 2 in Fig. 5.8.

$$V_{OMS1}\left(t = T_D - T_{CONS} + T_D - T_{SET}\right) = V_{HMIN} \quad \text{or}$$
$$V_{HMIN} = \left(V_{M11} A_1 e^{\frac{T_D - T_{CONS}}{\tau_{21}}} - V_{HMIN} \right) A_2 e^{\frac{T_D - T_{SET}}{\tau_{22}}} \tag{5.26}$$

From (5.26), the value of V_{M11} can be obtained by (5.27). This corresponds to the case when comparator 2 outputs logic "1".

$$V_{M11} = \left(V_{HMIN} + \frac{V_{HMIN}}{A_2} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \right) \frac{e^{-\frac{T_D - T_{CONS}}{\tau_{21}}}}{A_1} \tag{5.27}$$

Similarly, considering the other case when comparator 2 would output a logic "0" (bottom red dashed curve in the right side plot in Fig. 5.9), the value of input voltage

to comparator 1 (V_{M12}) that results in an output V_{M22} at time $t = T_D - T_{CONS}$ can be given as (5.28).

$$V_{M12} = \left(V_{HMIN} - \frac{|V_{LMAX}|}{A_2} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \right) \frac{e^{-\frac{T_D - T_{CONS}}{\tau_{21}}}}{A_1} \tag{5.28}$$

So, the total region of metastability for the SAR ADC when input to comparator 1 is above $V_{REF} = 0$ is given as V_{M2H} as shown in equation (5.29)

$$V_{M2H} = V_{M11} - V_{M12} \quad or$$

$$V_{M2H} = \frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{A_1 A_2} e^{-\frac{T_D - T_{CONS}}{\tau_{21}}} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \tag{5.29}$$

Similarly, the region of metastability for the SAR ADC when input to comparator 1 is below $V_{REF} = 0$ can be given as V_{M2L} in (5.30). In this case, comparator 3 is subject to metastability.

$$V_{M2L} = \frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{A_1 A_2} e^{-\frac{T_D - T_{CONS}}{\tau_{21}}} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \tag{5.30}$$

Hence, the total region of metastability of SAR ADC with a metastable detection circuit in determining first bit (V_{REF}=0) is given by (5.31)

$$V_{MD1} = V_{M2H} + V_{M2L} \quad or$$

$$V_{MD1} = 2\frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{A_1 A_2} e^{-\frac{T_D - T_{CONS}}{\tau_{21}}} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \tag{5.31}$$

Similarly, the region of metastability when determining i^{th} bit in Fig. 5.8 can be given as (5.32) since there are a total of 2^{i-1} possible reference voltages to compare.

$$V_{MDi} = 2^i \frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{A_1 A_2} e^{-\frac{T_D - T_{CONS}}{\tau_{21}}} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \tag{5.32}$$

The total region of metastability for the SAR ADC can be given as V_{MD} in (5.33)

$$V_{MD} = \sum_{i=1}^{N} V_{MDi} = 2\left(2^N - 1\right) \frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{A_1 A_2} e^{-\frac{T_D - T_{CONS}}{\tau_{21}}} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \tag{5.33}$$

From (5.33), the probability of metastability can be given as $P_{MS,D}$ using equation (5.34).

$$P_{MS,D} = 2\left(2^N - 1\right) \frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{2V_R A_1 A_2} e^{-\frac{T_D - T_{CONS}}{\tau_{21}}} e^{-\frac{T_D - T_{SET}}{\tau_{22}}} \tag{5.34}$$

C) Compare probability of Metastability for both ADCs

Using equations (5.23) and (5.34), the probability of metastability in both SAR ADCs can be compared. Here, both the ADCs are compared for the probability of metastability for a given power dissipation. Let 3P be the total power consumed by comparators in each SAR ADC. The comparator in Fig. 5.7 can burn a total of 3P power. Let us assume that the three comparators in Fig. 5.8 are identical. As a result, $\tau_{22} = \tau_{21}$ and $A_1 = A_2$. So, each comparator in Fig. 5.8 can burn a total of P power. Assuming linear increase in speed with power in comparators, the comparator in Fig. 5.7 can be assumed to be about 3 times faster than each of the comparators in Fig. 5.8. So, $\tau_{22} = 3\tau_1$.

Also, the gain in comparator 1 in Fig. 5.8 can be assumed to be equal to the gain in comparator in Fig. 5.7 ($A = A_1 = A_2$).

Using above conditions, the probability of metastability of SAR ADC in Fig. 5.7 can be given as $P_{MS,\ ADCP}$ and that of SAR ADC in Fig. 5.8 can be given as $P_{MS,DP}$ in equations (5.35) and (5.36) respectively.

$$P_{MS,ADCP} = \left(2^N - 1\right)\frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{2V_R A_2} e^{-\frac{3(T_D - T_{CONS})}{\tau_{22}}} \tag{5.35}$$

$$P_{MS,DP} = 2\left(2^N - 1\right)\frac{\left(|V_{LMAX}| + |V_{HMIN}|\right)}{2V_R A_2 A_2} e^{-\frac{2T_D - T_{SET} - T_{CONS}}{\tau_{22}}} \tag{5.36}$$

Fig. 5.10 shows the plots of $P_{MS,ADCP}$ and $P_{MS,DP}$ with respect to T_D. The value of τ_{22} is 120ps, A_2 is 50, T_{SET} is 100ps, N is 12 and T_{CONS} is 500ps. The time period of internal clock T_D is varied from 600ps to 2ns. From (5.18), it can be said that with decrease in T_D, the sampling clock period, T, also decreases. This results in increase in sampling clock speed. So, Fig. 5.10 shows the probability of metastability of both SAR ADCs with respect to increase in clock speed. As T_D decreases, the clock speed increases.

From Fig. 5.10, it can be said that, if the power dissipation is same in both the ADCs, as frequency of the clock decreases (that is as T_D increases), the probability of metastability of SAR ADC without using MSD circuit (Fig. 5.7) is better than that of the SAR ADC using MSD circuit (Fig. 5.8). This is because, the comparator in Fig. 5.7 is about three times faster than that of the comparators in Fig. 5.8 and there is sufficient

time available for the comparator in Fig. 5.7 to provide a valid logic output (as T_D is high). However, as the speed of sampling clock increases (that is as T_D decreases), the SAR ADC in Fig. 5.8 using a MSD circuit provides better probability of metastability. This can be explained as follows. As T_D decreases, there is metastability in comparator in Fig. 5.7 and comparator 1 in Fig. 5.8. However, due to the presence of the MSD circuit and the error correction block in Fig. 5.8, many of the metastable events are detected and corrected, thus providing smaller probability of metastability.

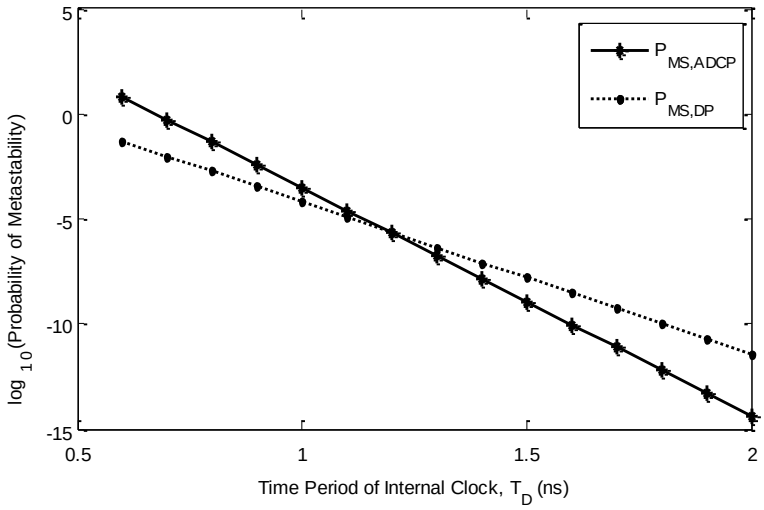

Figure 5.10: Probability of metastability of SAR ADC with (dashed, PMS,DP) and without (solid, PMS,ADCP) using metastable detection circuit for constant power dissipation.

From the above analysis and from Fig. 5.10, it can be said that using MSD circuit can decrease the probability of metastability in high speed synchronous SAR ADC

VI. CONCLUSION

A rigorous definition of metastability in comparators was provided along with a method to identify the maximum and minimum voltage values that determine valid logic levels. The probability of metastability in comparators with and without using inverters at the output of latch was analyzed. It was shown that if the time constant of comparator A is smaller than that of comparator B, the probability of metastability of comparator A is always smaller than that of comparator B. If time constant of comparator B is smaller than that of comparator A, there is a time point, T_P', until which comparator A has smaller probability of metastability. However, after this time T_P', the probability of metastability in comparator B is smaller than that of comparator A. Also, the probability of metastability in synchronous Successive Approximation Register ADCs with and without using a Metastable Detection circuit was analyzed. It was shown using mathematical analysis that as the frequency of clock increases, using MSD circuit decreases the probability of metastability in SAR ADCs.

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CHAPTER 6

SUMMARY

In this dissertation, the challenges associated with spectral testing of high performance ADCs and waveform generators were addressed. Three new methods were proposed that relax three of the stringent conditions required for spectral testing using standard methods. These stringent conditions are major contributors to the high costs associated with spectral testing. The first method, Fundamental Identification and Replacement (FIRE), completely eliminates the requirement of coherent sampling for spectral testing. The second method, Fundamental Estimation, Removal and Residue Interpolation (FERARI), relaxes the conditions to have precise control over amplitude and frequency of the input signal. The method can provide accurate spectral results from a non-coherently sampled and clipped data set. The third method simultaneously relaxes the conditions of coherent sampling and using a spectrally pure signal source as the input to the ADC to perform spectral testing. All of these methods decrease the test cost by enabling a low-cost, low-end measurement setup to test high performance ADCs. Furthermore, the methods can be used for BIST applications where high-end test circuitry cannot be practically designed for inclusion on-chip. Efficiency and robustness of the three proposed methods of testing were verified by using an ADC as the Device under Test. The proposed methods can also be used to test spectral characteristics of high performance waveform generators.

Finally, an analysis of the probability of metastability in comparators and SAR ADCs was presented. It was shown using this analysis that as the clock frequency of a

SAR ADC increases, it is favorable to use metastability detection circuit to decrease the probability of metastability.

APPENDIX

EQUATIONS TO OBTAIN THE JACOBEAN MATRIX IN CHAPTER 4 (4.33)

The equations to obtain the Jacobean matrix, *Jb*, in equation (4.36) are given in this appendix. It can be seen from equation (4.33) that for a given index k, if k is odd integer, f_k is obtained from the real part of $X_{g,k}$ (which is given as g_{rk}). Similarly, if k is an even integer, f_k is obtained from the imaginary part of $X_{g,k}$ (which is given as g_{ik}). So, to obtain expressions for all the 6H rows in (4.34), it is sufficient to obtain the partial derivatives of g_{rk} and g_{ik} (for generalized k) with respect to the parameters in matrix γ.

For odd subscripts of *f* (or odd values of index k), the partial derivatives of f_k (g_{rk}) with respect to A_1, δ, ϕ, β_h, α_h are provided below as (A.1 – A.5). (Here h varies from 2 to H).

$$\frac{\partial f_k}{\partial A_1} = \frac{\partial g_{rk}}{\partial A_1} = \frac{1}{4}\left(\begin{array}{l} \left[\sin\left(2\pi\delta+\phi\right)-\sin\left(\phi\right)\right]\left(\begin{array}{l} \cot\left(\dfrac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right) \\ +\cot\left(\dfrac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right) \end{array} \right) \\ +2\left[\cos\left(\phi\right)-\cos\left(2\pi\delta+\phi\right)\right] \end{array} \right) \tag{A.1}$$

$$\frac{\partial f_k}{\partial \alpha_h} = \frac{\partial g_{rk}}{\partial \alpha_h} = \frac{1}{4}\left(\begin{array}{l} \left\{ \left(\begin{array}{l} \left[\cos\left(h\phi\right)-\cos\left(h2\pi\delta+h\phi\right)\right]\left(\begin{array}{l} \cot\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right) \\ +\cot\left(\dfrac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right) \end{array} \right) \\ -2\left(\sin\left(h2\pi\delta+h\phi\right)-\sin\left(h\phi\right)\right) \end{array} \right) \right\} \end{array} \right) \tag{A.2}$$

$$\frac{\partial f_1}{\partial \beta_h} = \frac{\partial g_{rk}}{\partial \beta_h} = \frac{1}{4}\left\{\left\{\left\{\begin{array}{l}\left[\sin\left(h2\pi\delta + h\phi\right) - \sin\left(h\phi\right)\right]\left\{\begin{array}{l}\cot\left(\dfrac{\pi\left(hJ_{\text{int}} + h\delta - k\right)}{M}\right) \\ +\cot\left(\dfrac{\pi\left(hJ_{\text{int}} + h\delta + k\right)}{M}\right)\end{array}\right\} \\ +2\left(\cos\left(h\phi\right) - \cos\left(h2\pi\delta + h\phi\right)\right)\end{array}\right\}\right\} \qquad \text{(A.3)}$$

$$\frac{\partial f_k}{\partial \phi} = \frac{\partial g_{rk}}{\partial \phi} = \frac{A_1}{4}\left\{\begin{array}{l}\left[\cos\left(2\pi\delta + \phi\right) - \cos\left(\phi\right)\right]\left\{\begin{array}{l}\cot\left(\dfrac{\pi\left(J_{\text{int}} + \delta - k\right)}{M}\right) \\ +\cot\left(\dfrac{\pi\left(J_{\text{int}} + \delta + k\right)}{M}\right)\end{array}\right\} \\ +2\left(\sin\left(2\pi\delta + \phi\right) - \sin\left(\phi\right)\right)\end{array}\right\}$$

$$+\sum_{h=2}^{H}\left\{\begin{array}{l}\dfrac{\alpha_h}{4}\left\{\left\{\begin{array}{l}h\left[\sin\left(h2\pi\delta + h\phi\right) - \sin\left(h\phi\right)\right]\left\{\begin{array}{l}\cot\left(\dfrac{\pi\left(hJ_{\text{int}} + h\delta - k\right)}{M}\right) \\ +\cot\left(\dfrac{\pi\left(hJ_{\text{int}} + h\delta + k\right)}{M}\right)\end{array}\right\} \\ -2h\left(\cos\left(h2\pi\delta + h\phi\right) - \cos\left(h\phi\right)\right)\end{array}\right\}\right\} \\ +\dfrac{\beta_h}{4}\left\{\left\{\begin{array}{l}h\left[\cos\left(h2\pi\delta + h\phi\right) - \cos\left(h\phi\right)\right]\left\{\begin{array}{l}\cot\left(\dfrac{\pi\left(hJ_{\text{int}} + h\delta - k\right)}{M}\right) \\ +\cot\left(\dfrac{\pi\left(hJ_{\text{int}} + h\delta + k\right)}{M}\right)\end{array}\right\} \\ +2h\left(\sin\left(h2\pi\delta + h\phi\right) - \sin\left(h\phi\right)\right)\end{array}\right\}\right\}\end{array}\right\} \qquad \text{(A.4)}$$

$$\frac{\partial f_k}{\partial \delta}=\frac{\partial g_{rk}}{\partial \delta}=\frac{A_1}{4}\left(\begin{array}{l}\left[\sin\left(2\pi\delta+\phi\right)-\sin\left(\phi\right)\right]\left(\begin{array}{l}-\cos ec^2\left(\frac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)\\-\cos ec^2\left(\frac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)\end{array}\right)\left(\frac{\pi}{M}\right)\\+4\pi\left(\sin\left(2\pi\delta+\phi\right)\right)\\+\left[\cos\left(2\pi\delta+\phi\right)\right]\left(\begin{array}{l}\cot\left(\frac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)\\+\cot\left(\frac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)\end{array}\right)\left(2\pi\right)\end{array}\right)$$

$$+\sum_{h=2}^{H}\left(\begin{array}{l}\frac{\alpha_h}{4}\left\{\begin{array}{l}\left[\cos\left(h\phi\right)-\cos\left(h2\pi\delta+h\phi\right)\right]\left(\begin{array}{l}-\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\\-\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\end{array}\right)\left(\frac{h\pi}{M}\right)\\-4h\pi\left(\cos\left(h2\pi\delta+h\phi\right)\right)\\+\left(2\pi h\right)\left(\left[\sin\left(h2\pi\delta+h\phi\right)\right]\left(\begin{array}{l}\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\\+\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\end{array}\right)\right)\end{array}\right\}\\+\frac{\beta_h}{4}\left\{\begin{array}{l}\left[\sin\left(h2\pi\delta+h\phi\right)-\sin\left(h\phi\right)\right]\left(\begin{array}{l}-\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\\-\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\end{array}\right)\left(\frac{h\pi}{M}\right)\\+4h\pi\left(\sin\left(h2\pi\delta+h\phi\right)\right)\\+\left(2\pi h\right)\left(\left[\cos\left(h2\pi\delta+h\phi\right)\right]\left(\begin{array}{l}\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\\+\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\end{array}\right)\right)\end{array}\right\}\end{array}\right) \quad \text{(A.5)}$$

For even subscripts of f (or even values of index k), the partial derivatives of f_k (g_{ik}) with respect to A_1, δ, ϕ, β_h, α_h are provided below as (A.6 – A.10). (Here h varies from 2 to H).

$$\frac{\partial f_k}{\partial A_1} = \frac{\partial g_{ik}}{\partial A_1} = \frac{1}{4}\left(\left[\cos(\phi) - \cos(2\pi\delta + \phi)\right] \left(\begin{array}{l} \cot\left(\frac{\pi\left(J_{\text{int}} + \delta - k\right)}{M} \right) \\ -\cot\left(\frac{\pi\left(J_{\text{int}} + \delta + k\right)}{M} \right) \end{array} \right) \right) \tag{A.6}$$

$$\frac{\partial f_k}{\partial \alpha_h} = \frac{\partial g_{ik}}{\partial \alpha_h} = \left(-\frac{1}{4}\left[\sin(h2\pi\delta + h\phi) - \sin(h\phi)\right] \left(\begin{array}{l} \cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta - k\right)}{M} \right) \\ -\cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta + k\right)}{M} \right) \end{array} \right) \right) \tag{A.7}$$

$$\frac{\partial f_k}{\partial \beta_h} = \frac{\partial g_{ik}}{\partial \beta_h} = \left(\frac{1}{4}\left[\cos(h\phi) - \cos(h2\pi\delta + h\phi)\right] \left(\begin{array}{l} \cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta - k\right)}{M} \right) \\ -\cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta + k\right)}{M} \right) \end{array} \right) \right) \tag{A.8}$$

$$\frac{\partial f_k}{\partial \phi} = \frac{\partial g_{ik}}{\partial \phi} = \left(\begin{array}{l} \frac{A_1}{4}\left(\left[\sin(2\pi\delta + \phi) - \sin(\phi)\right] \left(\begin{array}{l} \cot\left(\frac{\pi\left(J_{\text{int}} + \delta - k\right)}{M} \right) \\ -\cot\left(\frac{\pi\left(J_{\text{int}} + \delta + k\right)}{M} \right) \end{array} \right) \right) \\ +\sum_{h=2}^{H} \left(\begin{array}{l} \frac{\beta_h}{4} h\left[\sin(h2\pi\delta + h\phi) - \sin(h\phi)\right] \left(\begin{array}{l} \cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta - k\right)}{M} \right) \\ -\cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta + k\right)}{M} \right) \end{array} \right) \\ -\frac{\alpha_h}{4} h\left[\cos(h2\pi\delta + h\phi) - \cos(h\phi)\right] \left(\begin{array}{l} \cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta - k\right)}{M} \right) \\ -\cot\left(\frac{\pi\left(hJ_{\text{int}} + h\delta + k\right)}{M} \right) \end{array} \right) \end{array} \right) \end{array} \right) \tag{A.9}$$

$$\frac{\partial f_k}{\partial \delta}=\frac{\partial g_{ik}}{\partial \delta}=\frac{A_1}{4}\left(\begin{array}{l}\left[\cos(\phi)-\cos(2\pi\delta+\phi)\right]\left(\begin{array}{l}\cos ec^2\left(\frac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)\\-\cos ec^2\left(\frac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)\end{array}\right)\left(\frac{\pi}{M}\right)\\+2\pi\left[\sin(2\pi\delta+\phi)\right]\left(\begin{array}{l}\cot\left(\frac{\pi\left(J_{\text{int}}+\delta-k\right)}{M}\right)\\-\cot\left(\frac{\pi\left(J_{\text{int}}+\delta+k\right)}{M}\right)\end{array}\right)\end{array}\right)$$

$$+\sum_{h=2}^{H}\left(\begin{array}{l}\frac{\beta_h}{4}\left(\begin{array}{l}\left[\cos(h\phi)-\cos(h2\pi\delta+h\phi)\right]\left(\begin{array}{l}\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\\-\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\end{array}\right)\left(\frac{h\pi}{M}\right)\\+2\pi h\left[\sin(h2\pi\delta+h\phi)\right]\left(\begin{array}{l}\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\\-\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\end{array}\right)\end{array}\right)\\-\frac{\alpha_h}{4}\left(\begin{array}{l}\left[\sin(h2\pi\delta+h\phi)-\sin(h\phi)\right]\left(\begin{array}{l}\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\\-\cos ec^2\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\end{array}\right)\left(\frac{h\pi}{M}\right)\\+2\pi h\left[\cos(h2\pi\delta+h\phi)\right]\left(\begin{array}{l}\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta-k\right)}{M}\right)\\-\cot\left(\frac{\pi\left(hJ_{\text{int}}+h\delta+k\right)}{M}\right)\end{array}\right)\end{array}\right)\end{array}\right) \quad \text{(A.10)}$$

Using the above equations for the values of k's in kSet (4.32) the Jacobean matrix, *Jb*, can be obtained.